



STB20N95K5, STF20N95K5 STP20N95K5, STW20N95K5

N-channel 950 V, 0.275 Ω , 17.5 A SuperMESH 5™ Power MOSFET
in D²PAK, TO-220FP, TO-220 and TO-247 packages

Datasheet — production data

Features

Order codes	V _{DSS}	R _{DS(on)} max	I _D	P _W
STB20N95K5	950 V	< 0.330 Ω	17.5 A	250 W
STF20N95K5				40 W
STP20N95K5				250 W
STW20N95K5				

- TO-220 worldwide best R_{DS(on)}
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using SuperMESH™ 5 technology. This revolutionary, avalanche-rugged, high voltage Power MOSFET technology is based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

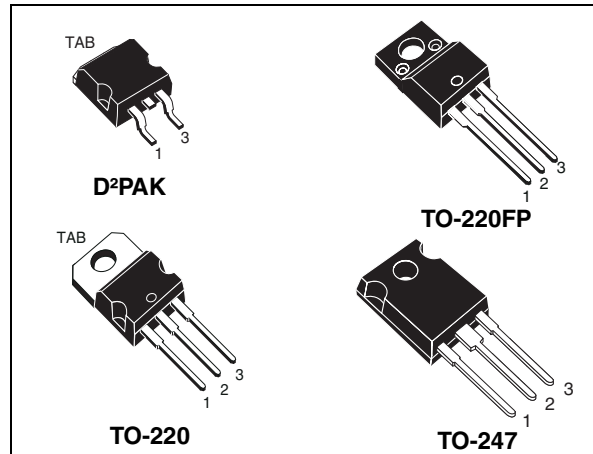


Figure 1. Internal schematic diagram

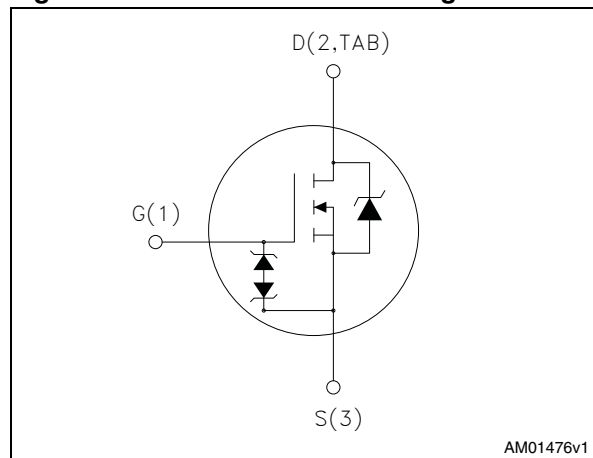


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB20N95K5	20N95K5	D ² PAK	Tape and reel
STF20N95K5		TO-220FP	Tube
STP20N95K5		TO-220	
STW20N95K5		TO-247	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK TO-220 TO-247	STF20N95K5	
V _{GS}	Gate- source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25 °C	17.5		A
I _D	Drain current (continuous) at T _C = 100 °C	11		A
I _{DM} ⁽¹⁾	Drain current (pulsed)	70		A
P _{TOT}	Total dissipation at T _C = 25 °C	250	40	W
I _{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T _{jmax})	6		A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D =I _{AS} , V _{DD} = 50 V)	200		mJ
ESD	Gate-source human body model (R= 1,5 kΩ C = 100 pF)	2		kV
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T _C =25 °C)	2500		V
dv/dt ⁽²⁾	Peak diode recovery voltage slope	6		V/ns
T _j T _{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Pulse width limited by safe operating area.

2. I_{SD} ≤ 17.5 A, di/dt ≤ 100 A/μs, V_{Peak} ≤ V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		D ² PAK	TO-220	TO-247	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	0.5			3.1	°C/W
R _{thj-amb}	Thermal resistance junction-amb max		62.5	50	62.5	°C/W
R _{thj-pcb}	Thermal resistance junction-pcb max	30				°C/W

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	950			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 950\text{ V},$ $V_{DS} = 950\text{ V}, T_c = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$		0.275	0.330	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$		1500		pF
C_{oss}	Output capacitance		-	80	-	pF
C_{rss}	Reverse transfer capacitance				5	
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0\text{ to }760\text{ V}$	-	170	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	65	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	3.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 760\text{ V}, I_D = 9\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 19)		40		nC
Q_{gs}	Gate-source charge		-	8	-	nC
Q_{gd}	Gate-drain charge				25	

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475 \text{ V}$, $I_D = 9 \text{ A}$, $R_G = 4.7 \text{ } \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 21)		17		ns
t_r	Rise time			12		ns
$t_{d(off)}$	Turn-off delay time			70		ns
t_f	Fall time			20		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				17.5	mA
I_{SDM}	Source-drain current (pulsed)				70	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 17.5 \text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 17.5 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, (see Figure 20)		530		ns
Q_{rr}	Reverse recovery charge			12		μC
I_{RRM}	Reverse recovery current			44		A
t_{rr}	Reverse recovery time	$I_{SD} = 17.5 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 20)		650		ns
Q_{rr}	Reverse recovery charge			14		μC
I_{RRM}	Reverse recovery current			44		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{gs} \pm 1 \text{ mA}$, ($I_D = 0$)	30	-	-	V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK and TO-220

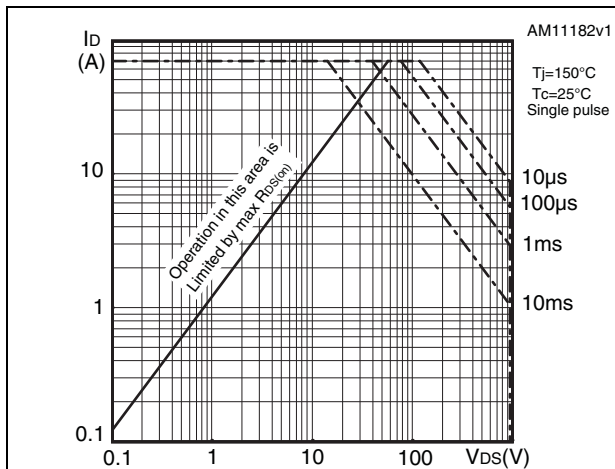


Figure 3. Thermal impedance for D²PAK and TO-220

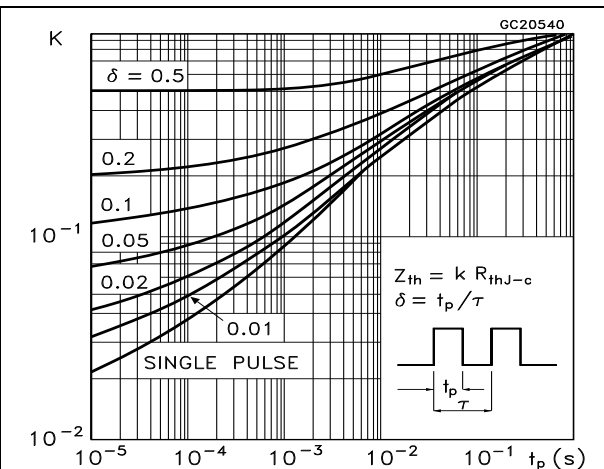


Figure 4. Safe operating area for TO-220FP

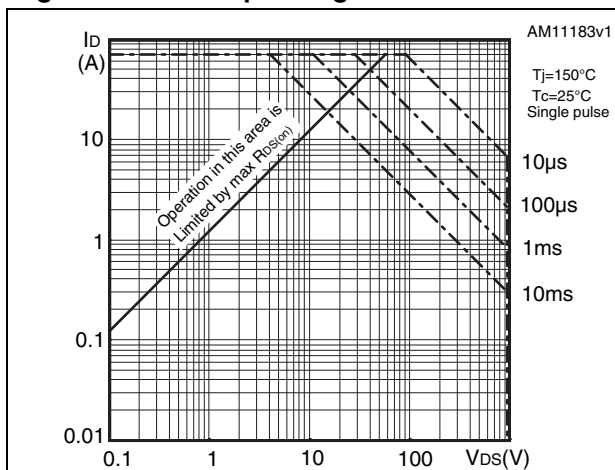


Figure 5. Thermal impedance for TO-220FP

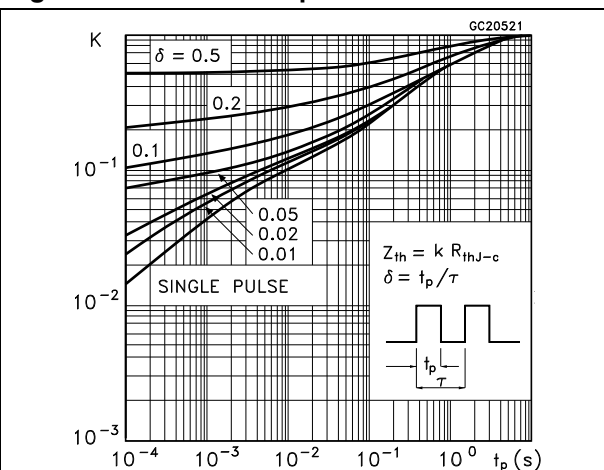


Figure 6. Safe operating area for TO-247

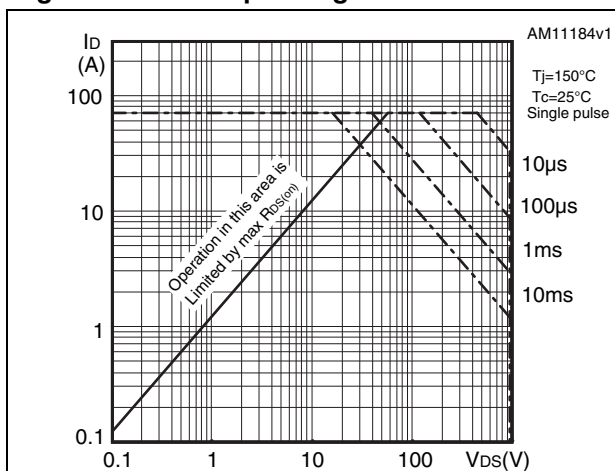


Figure 7. Thermal impedance for TO-247

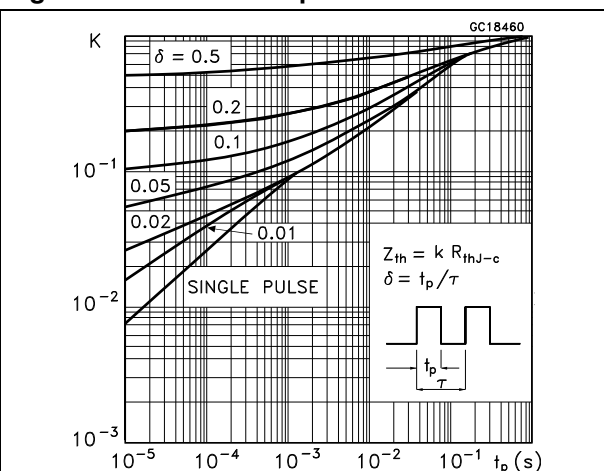


Figure 8. Output characteristics

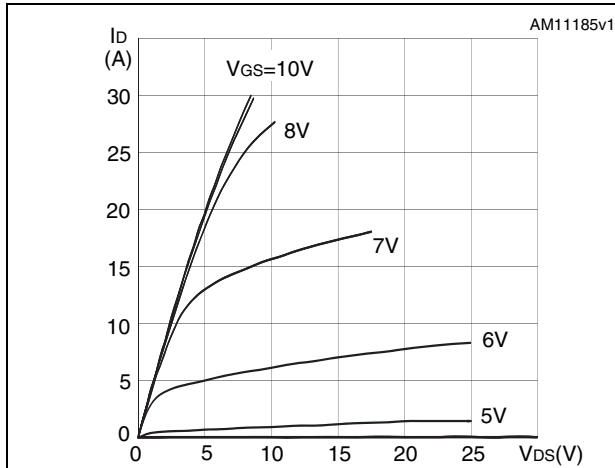


Figure 9. Transfer characteristics

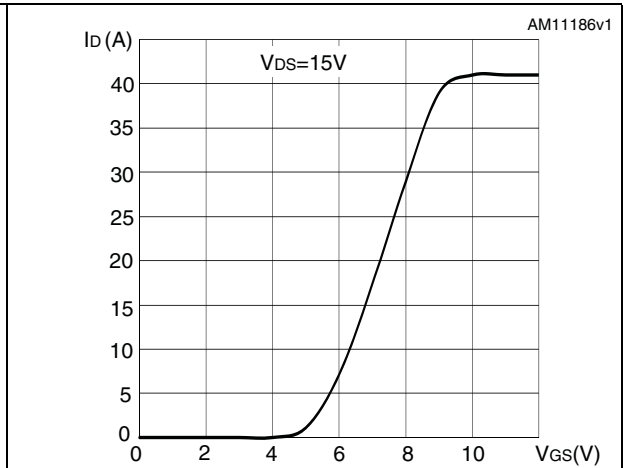


Figure 10. Gate charge vs gate-source voltage Figure 11. Static drain-source on-resistance

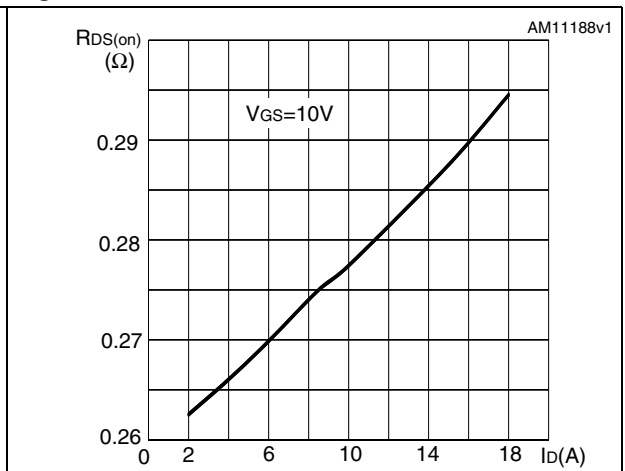
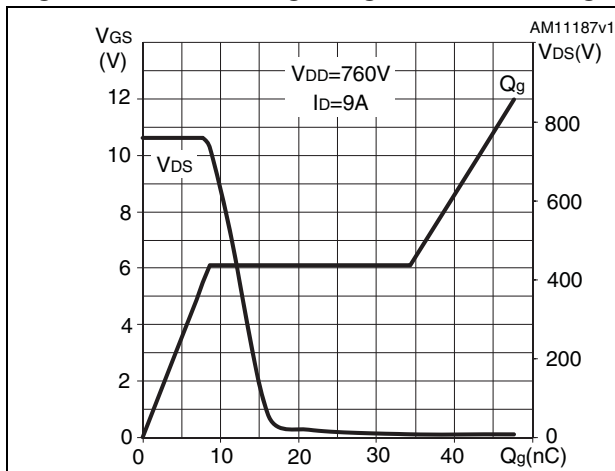


Figure 12. Capacitance variations

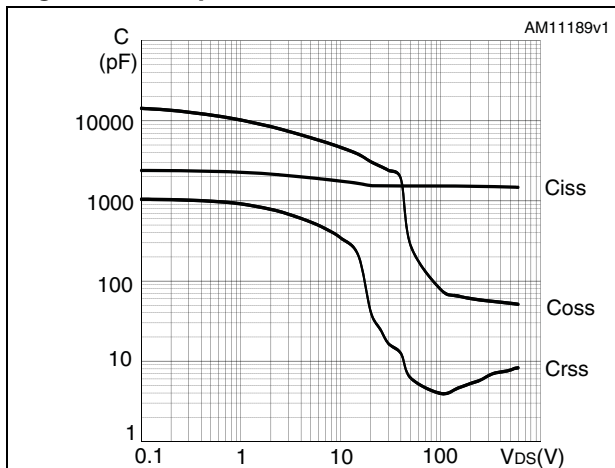


Figure 13. Output capacitance stored energy

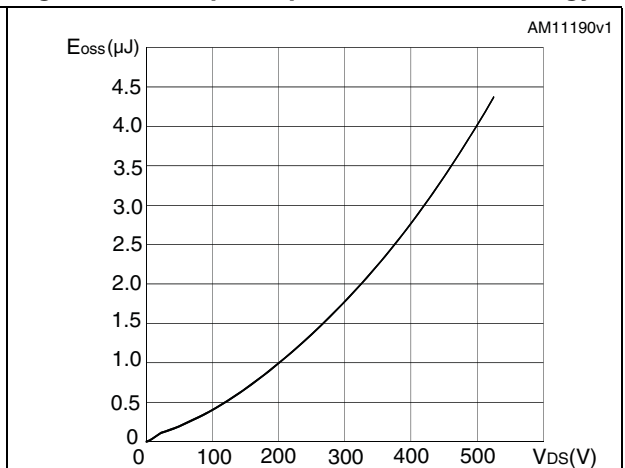


Figure 14. Normalized gate threshold voltage vs temperature

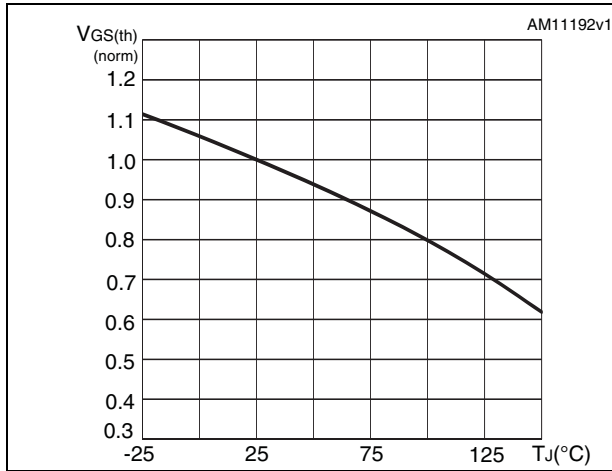


Figure 15. Normalized on-resistance vs temperature

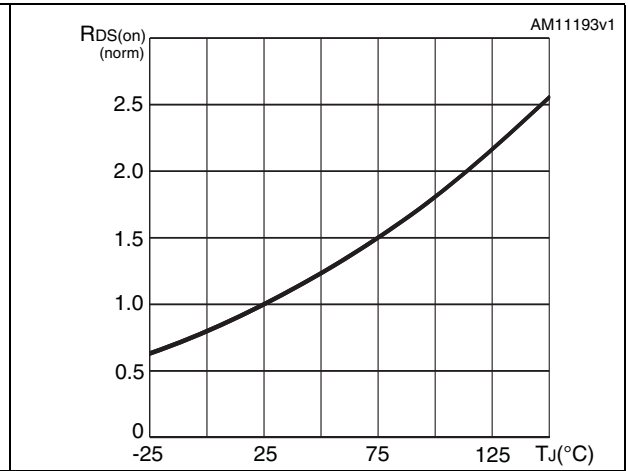


Figure 16. Maximum avalanche energy vs starting Tj

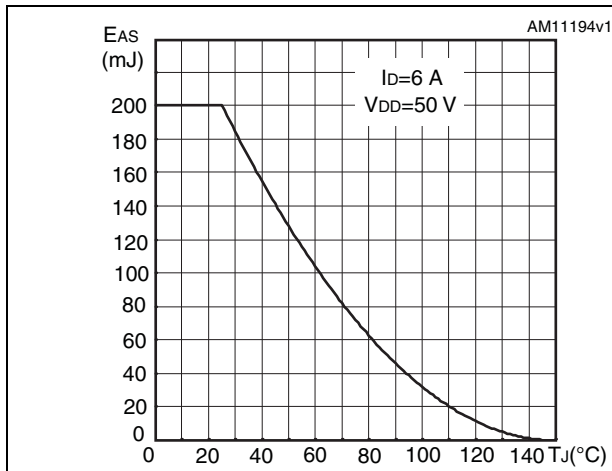
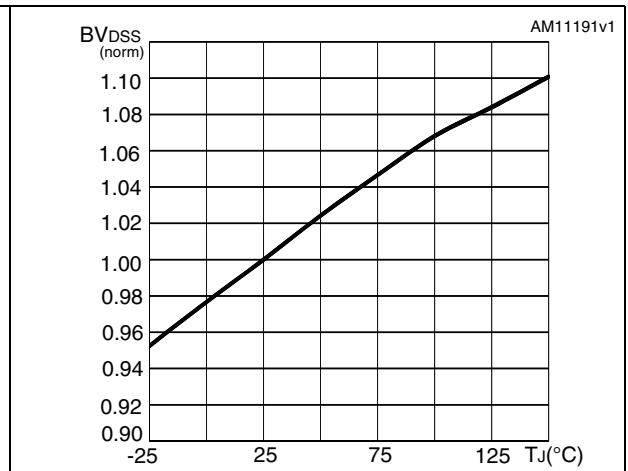


Figure 17. Normalized B_{VDSS} vs temperature



3 Test circuits

Figure 18. Switching times test circuit for resistive load



AM01468v1

Figure 19. Gate charge test circuit



AM01469v1

Figure 20. Test circuit for inductive load switching and diode recovery times



AM01470v1

Figure 21. Unclamped inductive load test circuit



AM01471v1

Figure 22. Unclamped inductive waveform



AM01472v1

Figure 23. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 24. D²PAK (TO-263) drawing

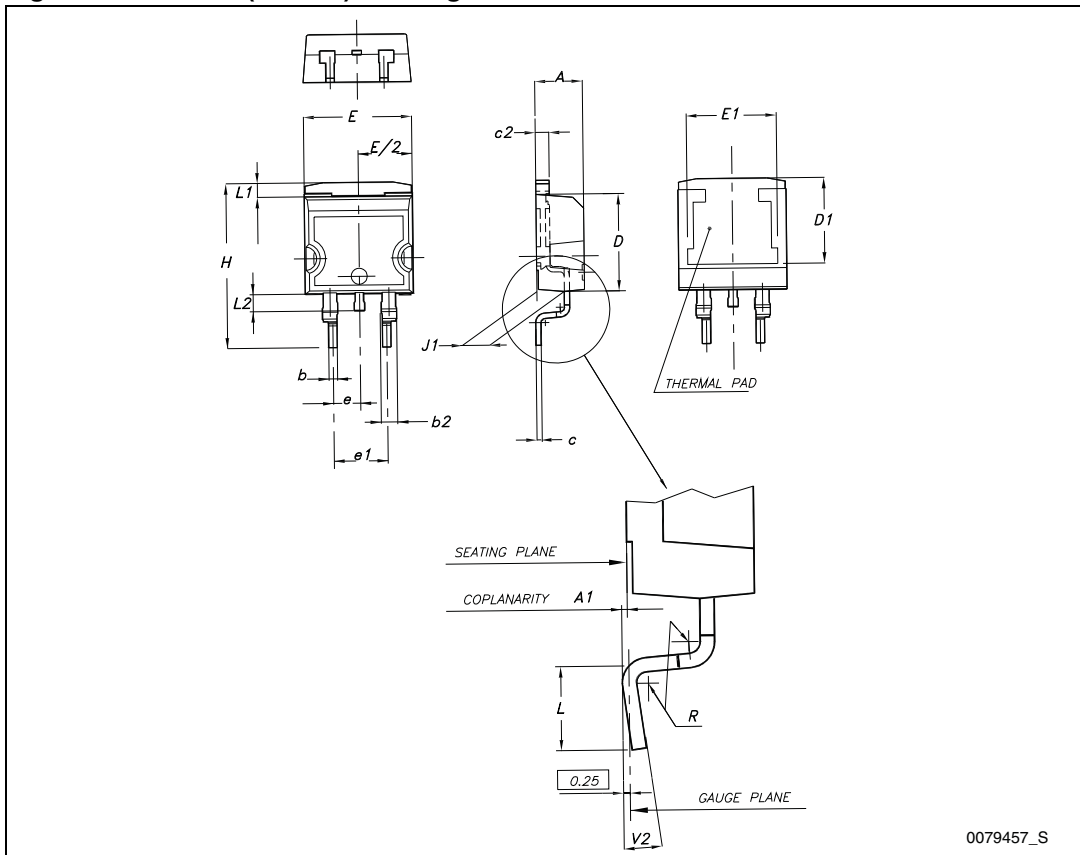


Figure 25. D²PAK footprint^(a)

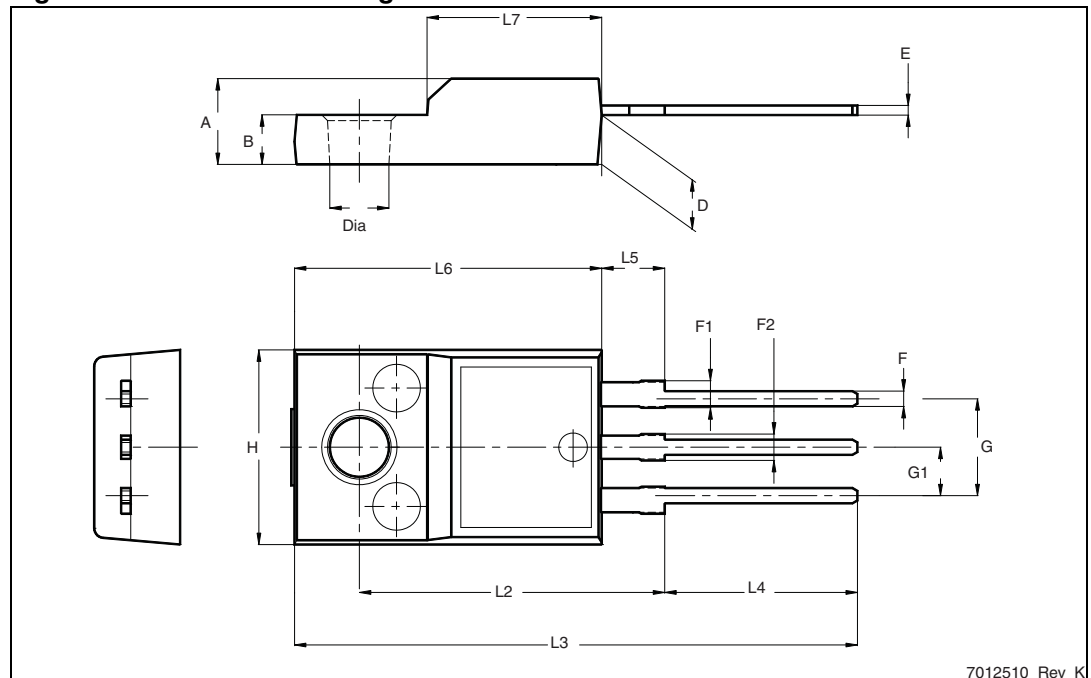


a. All dimensions are in millimeters

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 26. TO-220FP drawing



7012510 Rev K

Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing

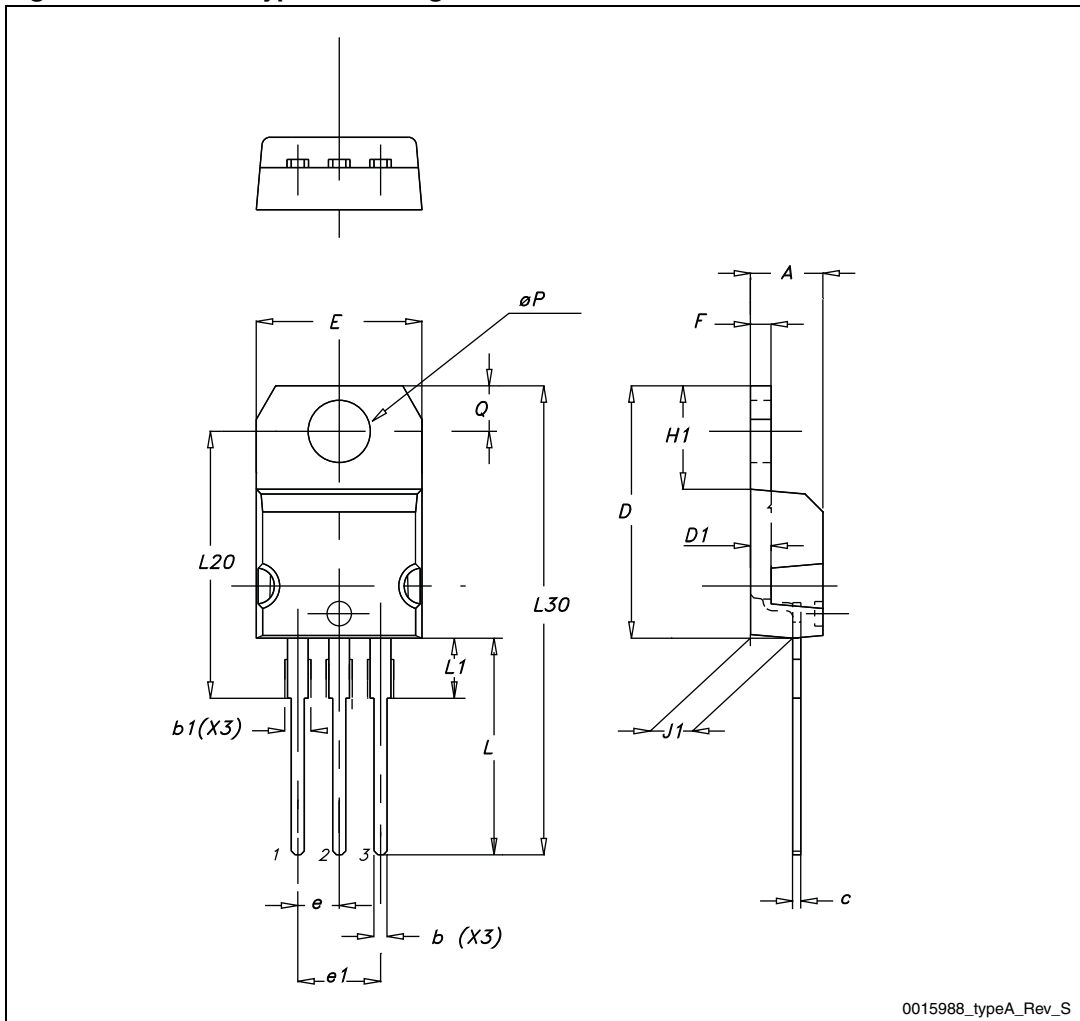
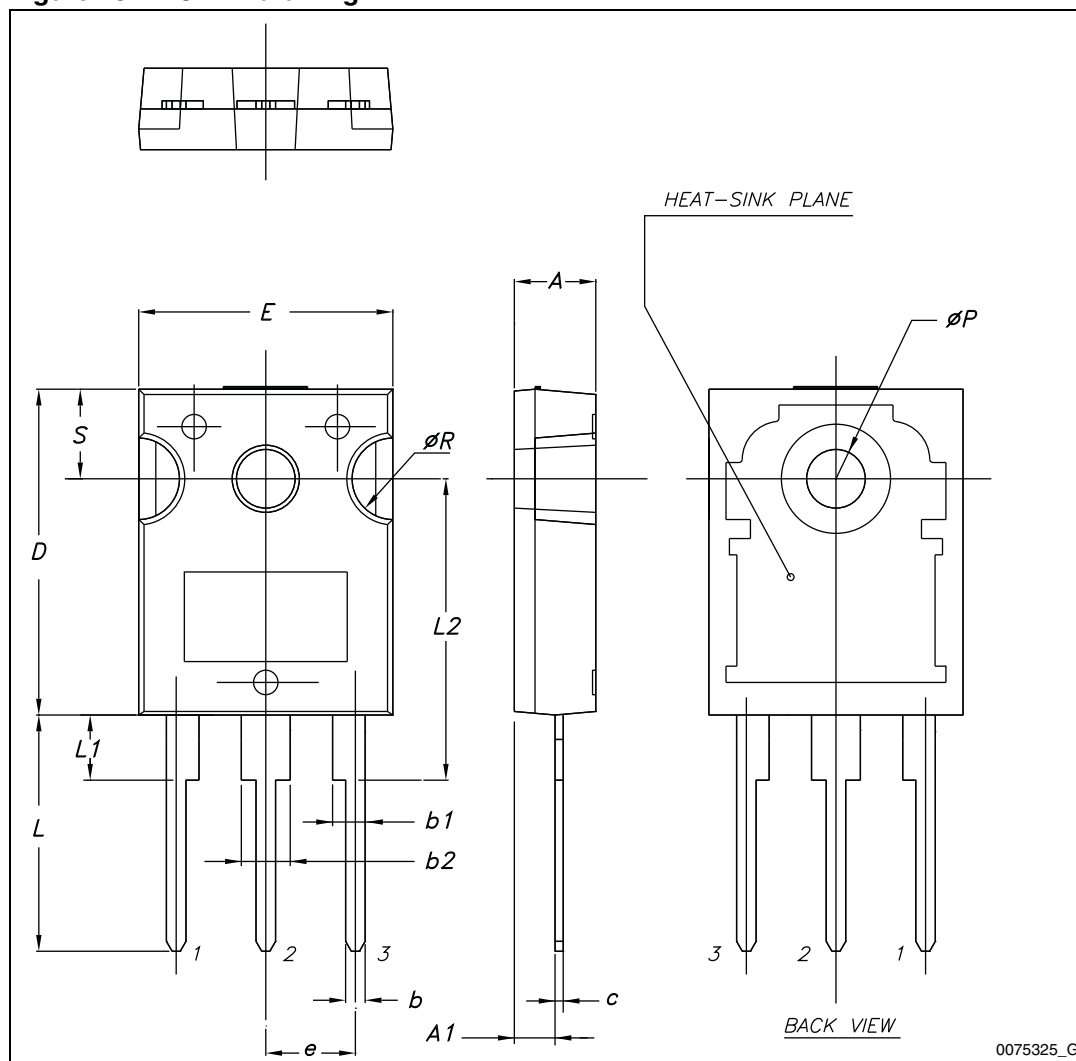


Table 12. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 28. TO-247 drawing



0075325_G

5 Packaging mechanical data

Table 13. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 29. Tape

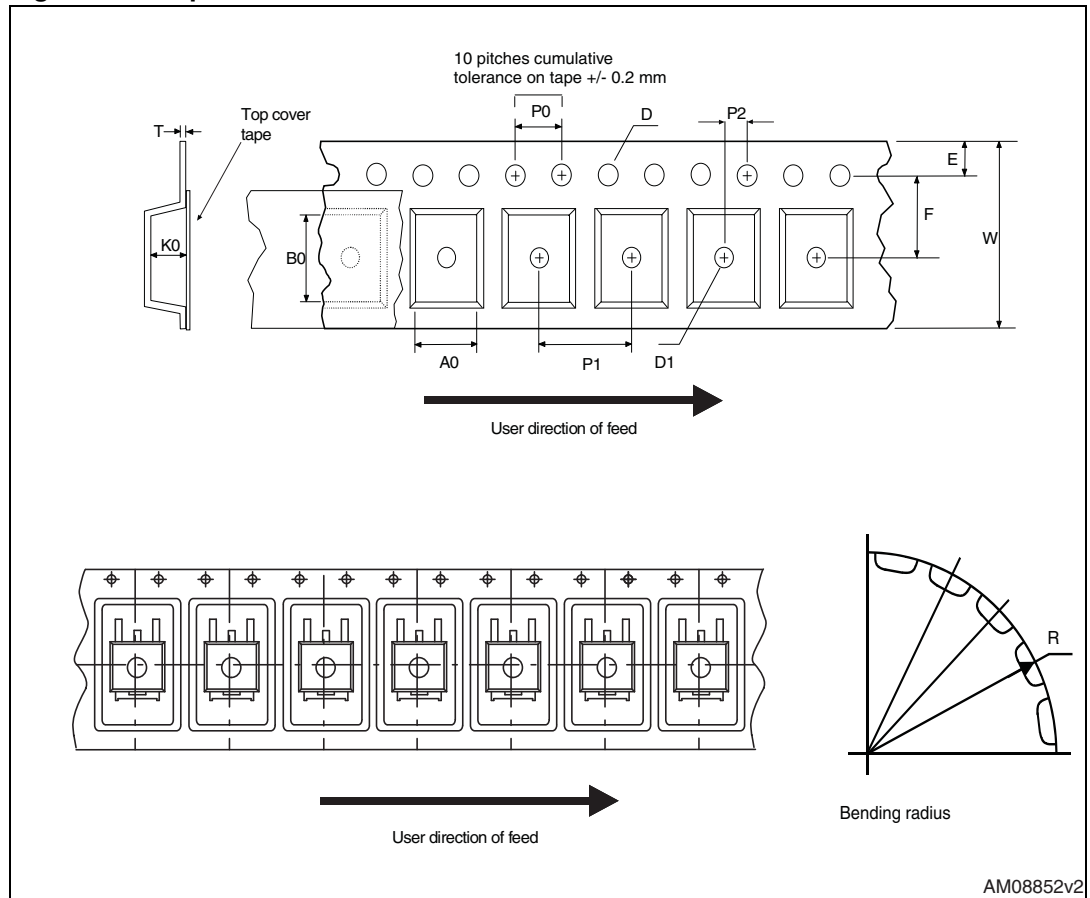
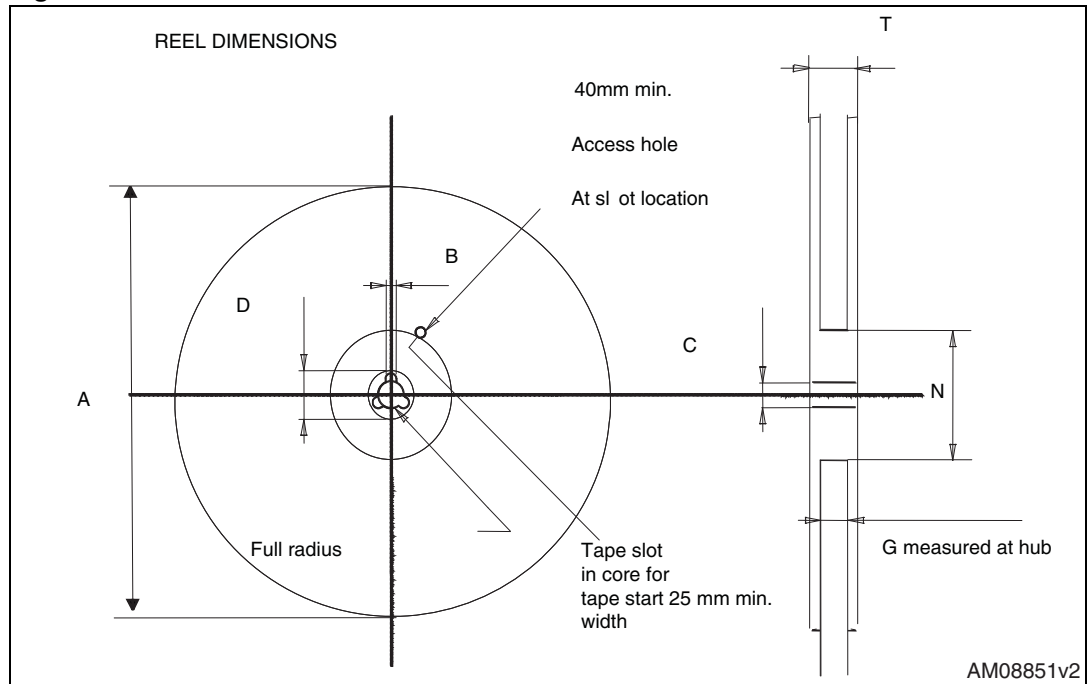


Figure 30. Reel



6 Revision history

Table 14. Document revision history

Date	Revision	Changes
25-Nov-2009	1	First release.
12-Jan-2010	2	Corrected V_{GS} value in Table 2: Absolute maximum ratings .
22-Dec-2011	3	Inserted device in D ² PAK. Document status promoted from preliminary data to datasheet. Added: Section 2.1: Electrical characteristics (curves) Updated Section 4: Package mechanical data . Added Section 5: Packaging mechanical data . Minor text changes.
06-Jun-2012	4	Figure 9: Transfer characteristics has been updated.

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