

2SC3844

Silicon High Speed Power Transistor

2SC3844 450V, 15A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Storage Temperature Range	T_{stg}		-55 ~ +150	°C
Junction Temperature	T_J		+150	°C
Collector to Base Voltage	V_{CBO}		600	V
Emitter to Base Voltage	V_{EBO}		7	V
Collector to Emitter Voltage	V_{CEO}		450	V
Collector Current	I_C		15	A
	I_{CM}	$P_W \leq 10ms, D.R. \leq 2\%$	20	
Base Current	I_B		5	A
Collector Power Dissipation	P_C	$T_C = 25^\circ C$	75	W

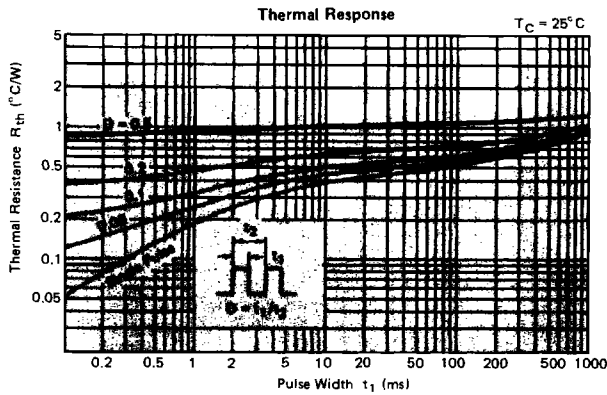
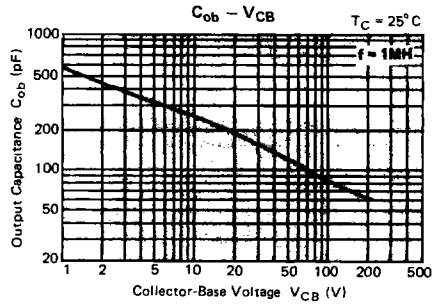
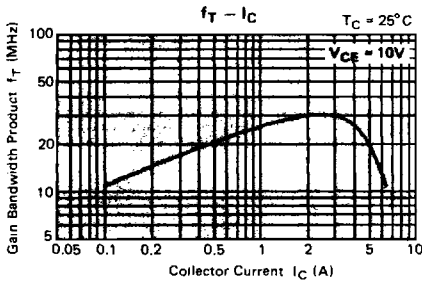
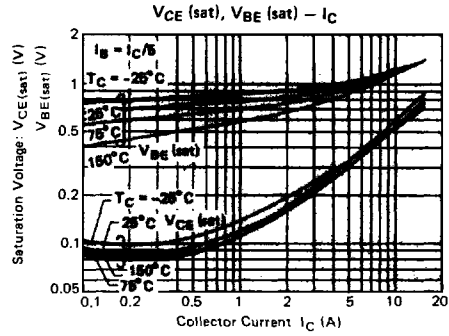
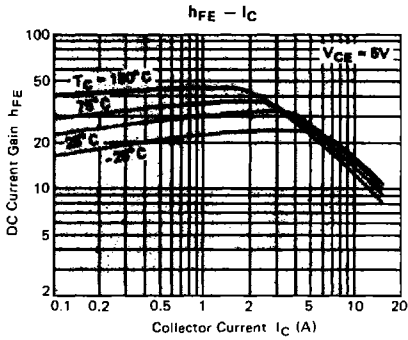
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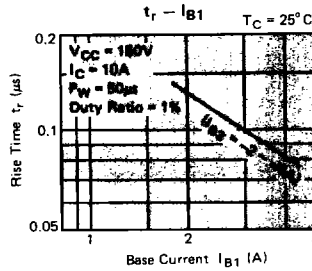
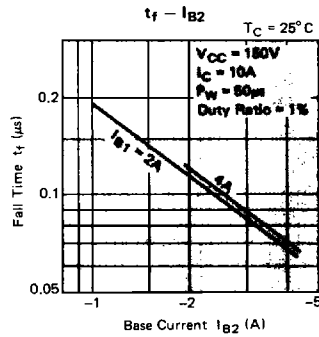
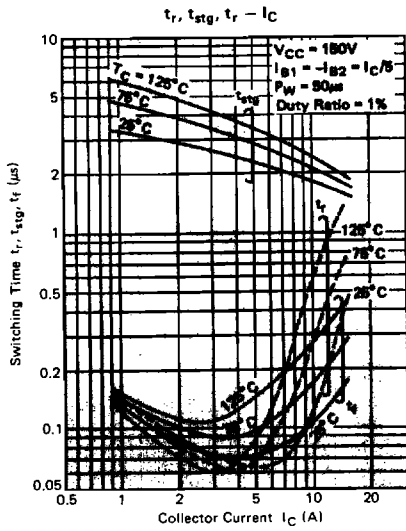
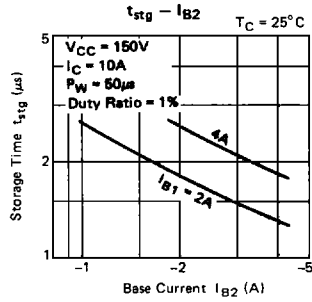
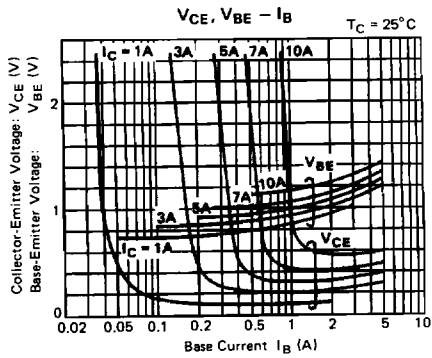
ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA, I_E = 0$	600	-	-	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA, I_C = 0$	7	-	-	V
Collector to Emitter Sustaining Voltage	$V_{CEO(SUS)}$	$I_C = 0.8A, R_{BE} = \infty\Omega$	450	-	-	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 8A, I_{B2} = -1A, L = 200\mu H^*$	450	-	-	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 500V, I_E = 0$	-	-	100	μA
		$V_{CB} = 500V, I_E = 0, T_C = 100^\circ C$	-	-	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V, I_C = 0$	-	-	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V, I_C = 10A^{**}$	10	15	30	-
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10A, I_B = 2A^{**}$	-	0.56	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		-	1.2	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0, f = 1MHz$	-	240	-	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 2A$	-	30	-	MHz
Rise Time	t_r	$V_{CC} = 150V, I_C = 10A, I_{B1} = -I_{B2} = 2A^*$	-	0.13	0.5	μs
Storage Time	t_{stg}		-	1.80	2.5	μs
Fall Time	t_f		-	0.11	0.3	μs

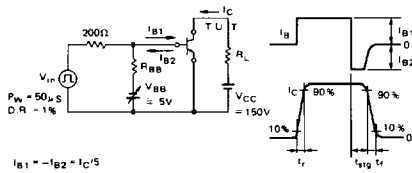
*1 Test Circuit **2 Pulse $P_W \leq 300\mu s$, Duty Ratio $\leq 6\%$

2



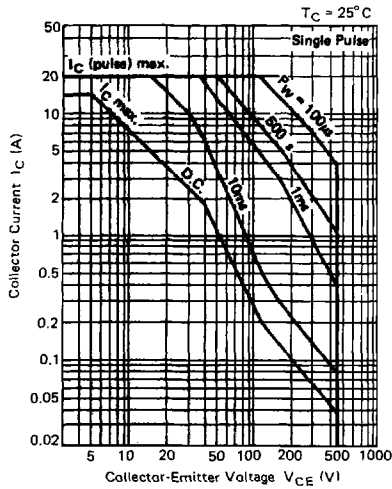


Test Circuit for Switching Time

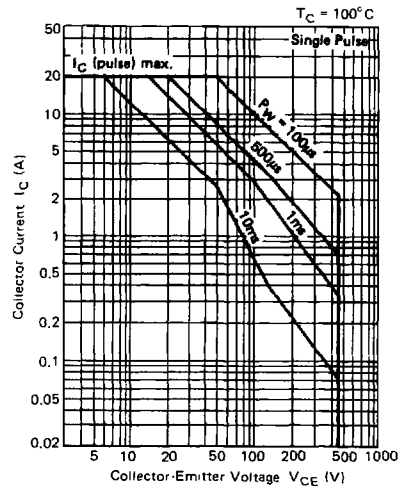


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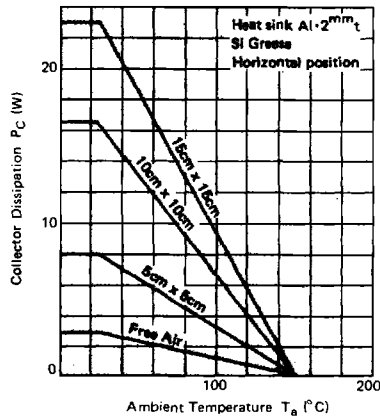
Forward Bias Safe Operating Area - 1



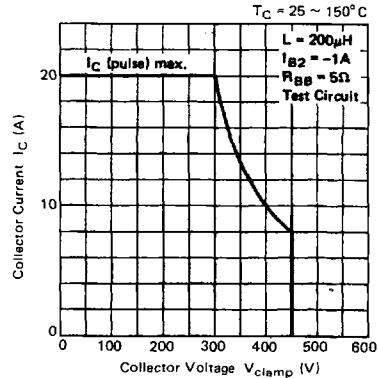
Forward Bias Safe Operating Area - 2



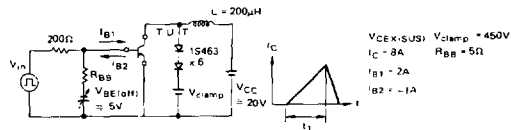
Pc - Ta



Reverse Bias Safe Operating Area



Test Circuit for VCEX(sus) and Reverse Bias Safe Operating Area



$$t_1 = \frac{L \cdot I_C}{V_{CC}}$$