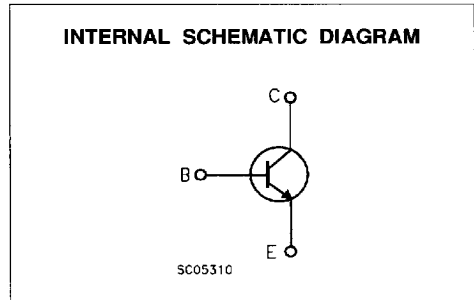
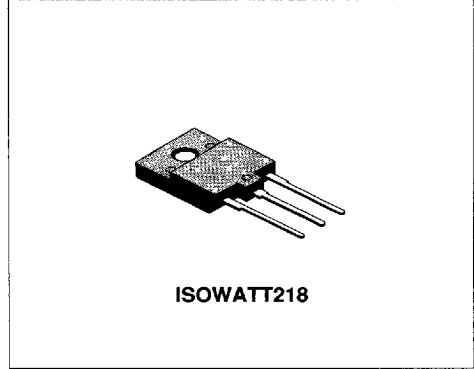


## CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- FULLY INSULATED PACKAGE FOR EASY MOUNTING
- LOW SATURATION VOLTAGE
- HIGH SWITCHING SPEED
- COMPLETE CHARACTERIZATION OF POWER LOSSES AND SWITCHING TIMES AS A FUNCTION OF NEGATIVE BASE CURRENT FOR OPTIMUM DRIVE

**APPLICATIONS:**

- HORIZONTAL DEFLECTION STAGE IN STANDARD AND HIGH RESOLUTION DISPLAYS FOR TV'S AND MONITORS
- SWITCHING POWER SUPPLY FOR TV'S AND MONITORS


**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CBO}$	Collector-Base Voltage ( $I_E = 0$ )	1700	V
$V_{CEO}$	Collector-Emitter Voltage ( $I_B = 0$ )	700	V
$V_{EBO}$	Emitter-Base Voltage ( $I_C = 0$ )	10	V
$I_C$	Collector Current	8	A
$I_{CM}$	Collector Peak Current ( $t_p < 5$ ms)	15	A
$I_B$	Base Current	5	A
$I_{BM}$	Base Peak Current ( $t_p < 5$ ms)	8	A
$P_{tot}$	Total Dissipation at $T_c = 25$ °C	60	W
$T_{stg}$	Storage Temperature	-65 to 150	°C
$T_J$	Max. Operating Junction Temperature	150	°C

**THERMAL DATA**

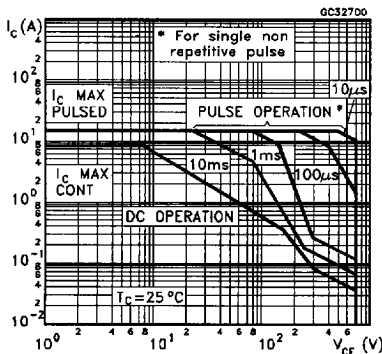
R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	2.08	°C/W
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**ELECTRICAL CHARACTERISTICS** (T<sub>case</sub> = 25 °C unless otherwise specified)

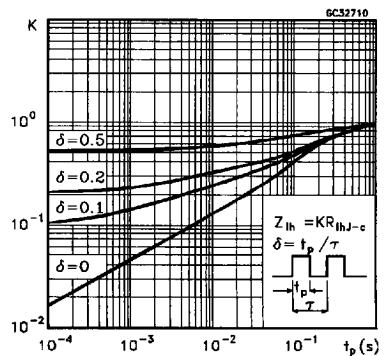
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I <sub>CES</sub>	Collector Cut-off Current (V <sub>BE</sub> = 0)	V <sub>CE</sub> = 1700 V V <sub>CE</sub> = 1700 V T <sub>J</sub> = 125 °C			1 2	mA mA
I <sub>EBO</sub>	Emitter Cut-off Current (I <sub>C</sub> = 0)	V <sub>EB</sub> = 5 V			100	μA
V <sub>CEO(sus)</sub>	Collector-Emitter Sustaining Voltage	I <sub>C</sub> = 100 mA	700			V
V <sub>EBO</sub>	Emitter-Base Voltage (I <sub>C</sub> = 0)	I <sub>E</sub> = 10 mA	10			V
V <sub>CE(sat)*</sub>	Collector-Emitter Saturation Voltage	I <sub>C</sub> = 5 A I <sub>B</sub> = 1.25 A			1.5	V
V <sub>BE(sat)*</sub>	Base-Emitter Saturation Voltage	I <sub>C</sub> = 5 A I <sub>B</sub> = 1.25 A			1.3	V
h <sub>FE*</sub>	DC Current Gain	I <sub>C</sub> = 5 A V <sub>CE</sub> = 5 V I <sub>C</sub> = 5 A V <sub>CE</sub> = 5 V T <sub>J</sub> = 100 °C	6 4			
t <sub>s</sub> t <sub>f</sub>	RESISTIVE LOAD Storage Time Fall Time	V <sub>CC</sub> = 400 V I <sub>C</sub> = 5 A I <sub>B1</sub> = 1.25 A I <sub>B2</sub> = 2.5 A		2.7 190	3.9 280	μs ns
t <sub>s</sub> t <sub>f</sub>	INDUCTIVE LOAD Storage Time Fall Time	I <sub>C</sub> = 5 A f = 15625 Hz I <sub>B1</sub> = 1.25 A I <sub>B2</sub> = 2.5 A V <sub>ceflyback</sub> = 1050 sin(π/10 10 <sup>6</sup> ) t V		2.3 350		μs ns
t <sub>s</sub> t <sub>f</sub>	INDUCTIVE LOAD Storage Time Fall Time	I <sub>C</sub> = 5 A f = 31250 Hz I <sub>B1</sub> = 1.25 A I <sub>B2</sub> = 2.5 A V <sub>ceflyback</sub> = 1200 sin(π/5 10 <sup>6</sup> ) t V		2.3 200		μs ns

\* Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %

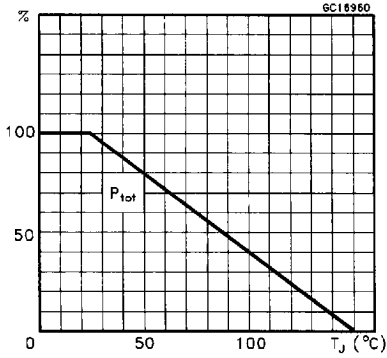
**Safe Operating Areas**



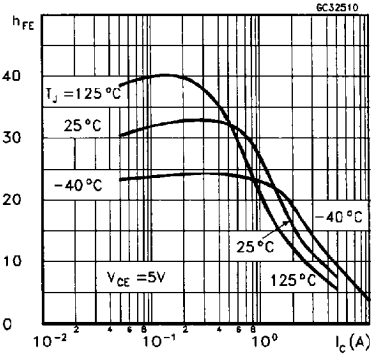
**Thermal Impedance**



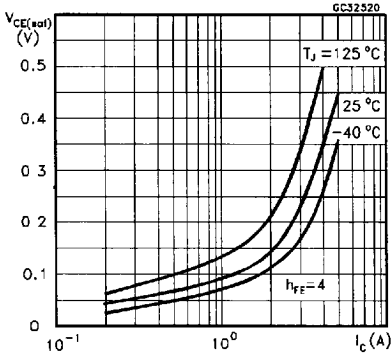
Derating Curves



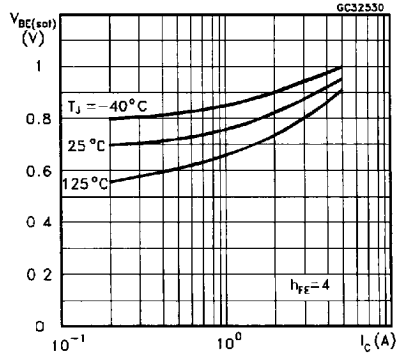
DC Current Gain



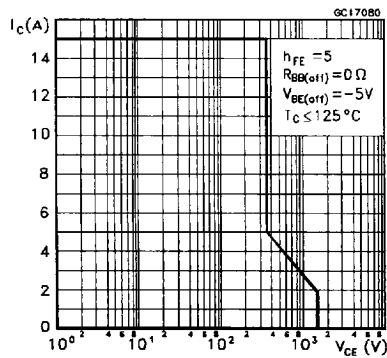
Collector-Emitter Saturation Voltage



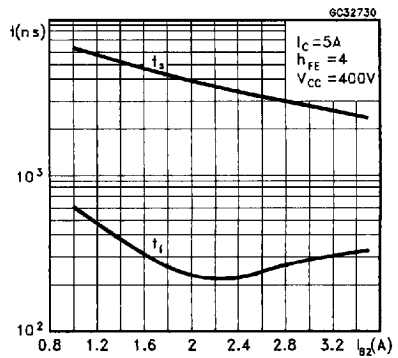
Base-Emitter Saturation Voltage



Reverse Biased SOA

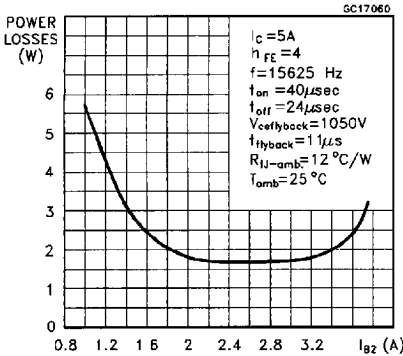


Switching Time Resistive Load

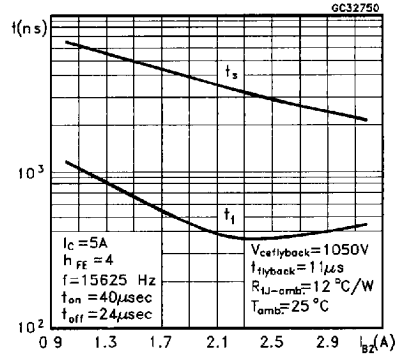


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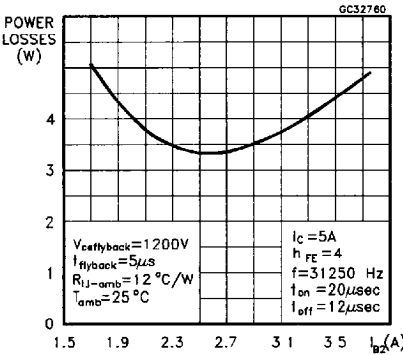
Power Losses at 16 KHz



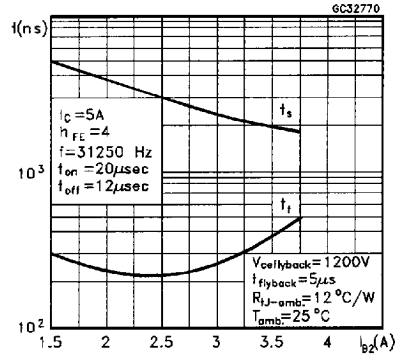
Switching Time Inductive Load at 16 KHz (see figure 2)



Power Losses at 32 KHz



Switching Time Inductive Load at 32 KHz (see figure 2)



BASE DRIVE INFORMATION

A fundamental parameter of high voltage power transistors like those used in the horizontal deflection stage is their junction temperature  $T_J$ , which, in turn, depends on the power dissipation. This parameter turns out to influence the system reliability under normal operation. Based on that, SGS-THOMSON has introduced a new dynamic, application-oriented characterization differing from the traditional data given in most datasheets.

In order to saturate the power switch and reduce conduction losses, adequate direct base current  $I_{B1}$  has to be provided for the lowest gain  $h_{FE}$  at  $T_J = 100 \text{ }^\circ\text{C}$  (line scan phase). On the other hand, negative base current  $I_{B2}$  must be provided for

the transistor to be turned off (retrace phase). Most of the dissipation, especially in the deflection application, occurs at switch-off so it is essential to determine the value of  $I_{B2}$  which minimizes power losses, fall time  $t_f$  and, consequently,  $T_J$ . A new set of curves have been defined to give total power losses,  $t_s$  and  $t_f$  as a function of  $I_{B2}$  at both 16 KHz and 32 KHz scanning frequencies for choosing the optimum negative drive. The test circuit is illustrated in fig. 1.

Inductance  $L_1$  serves to control the slope of the negative base current  $I_{B2}$  in order that excess carriers in the collector recombine when base current is still present, thus avoiding any tailing phenomenon in the collector current. This effect

is, in any case, markedly reduced intrinsically by adopting the hollow emitter technology. The values of L and C are calculated from the following equations:

$$\frac{1}{2} L (I_c)^2 = \frac{1}{2} C (V_{CEfly})^2$$

$$\omega = 2 \pi f = \frac{1}{\sqrt{LC}}$$

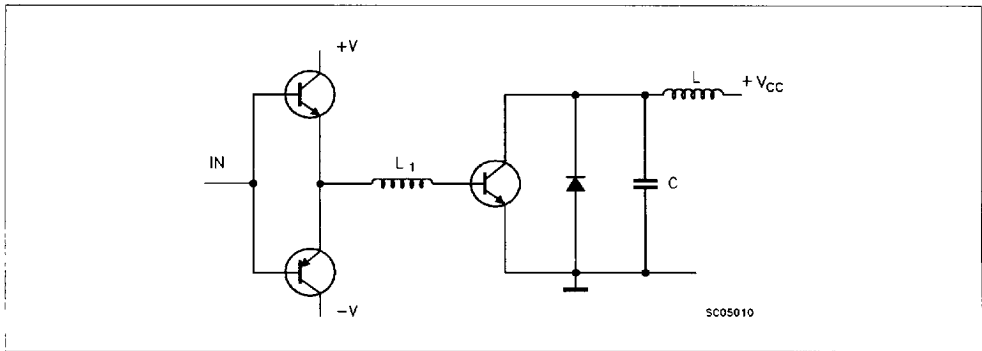
Where  $I_c$  = operating collector current,  $V_{CEfly}$  = flyback voltage,  $f$  = frequency of oscillation during retrace.

**RBSOA INFORMATION**

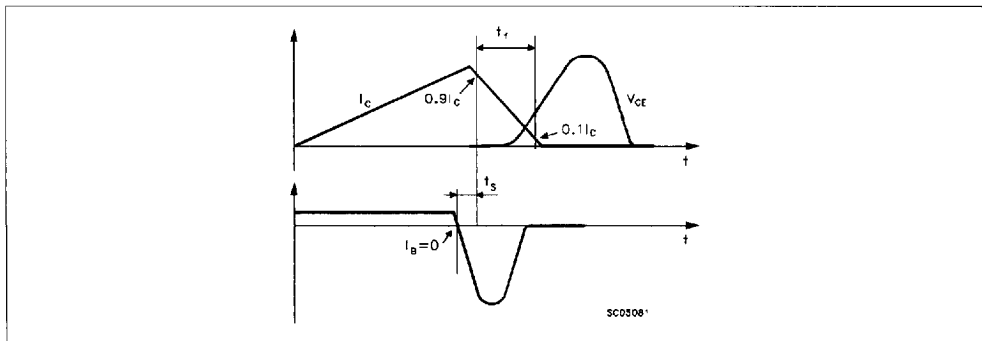
During turn-off with an inductive load, the power transistor has to withstand high voltages and high currents simultaneously with negative base-to-emitter voltage  $V_{BEoff}$ . Very often it has to reach a working area above  $V_{CE0}$ , remaining there all the time needed for the collector current  $I_c$  to fall to zero. The safe operation for the power transistor under these conditions is specified by RBSOA (Reverse Bias Safe Operating Area) which repre-

sents the permissible  $I_c$ - $V_{CE}$  locus within which proper operation is guaranteed. RBSOA is strongly dependent on the circuit topology and is valid only under specified drive conditions. High voltage Multiepitaxial Fastswitching transistors of the BUH series have been optimized to give improved RBSOA to suit off-line switch mode power supplies applications.

**Figure 1: Test Circuits for Dynamic Characterization.**



**Figure 2: Switching Waveforms in a Deflection Circuit**



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