

# DATA SHEET

## **BS107A**

N-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# N-channel enhancement mode vertical D-MOS transistor

**BS107A**

**FEATURES**

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

**DESCRIPTION**

N-channel enhancement mode vertical D-MOS transistor in TO-92 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

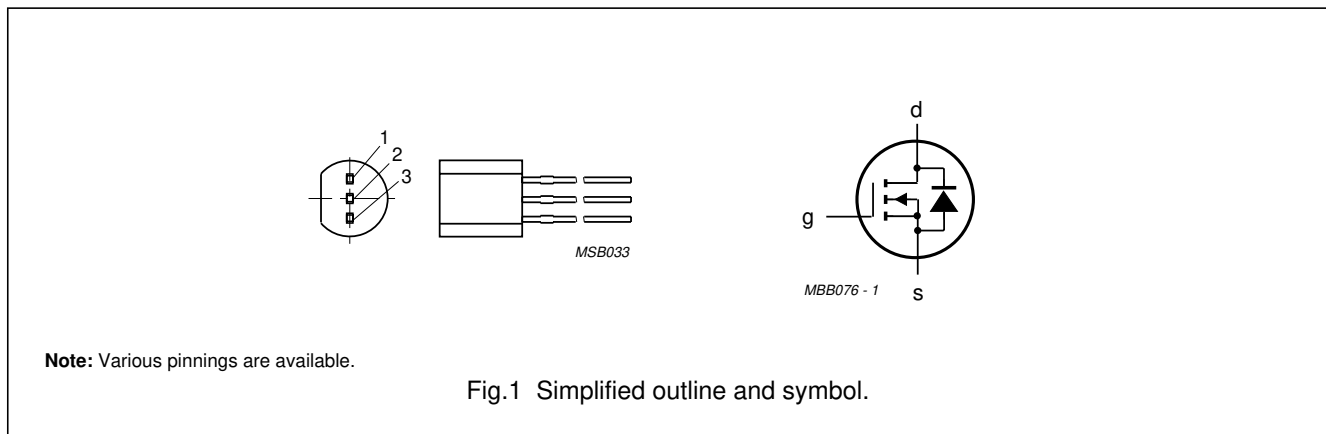
**QUICK REFERENCE DATA**

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	250 mA
Total power dissipation up to $T_{case} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	0.6 W
Drain-source ON-resistance $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ.	4.5 $\Omega$
		max.	6.4 $\Omega$
Transfer admittance $I_D = 250\text{ mA}; V_{GS} = 25\text{ V}$	$ Y_{fs} $	min.	200 mS
		typ.	350 mS

**PINNING - TO-92**

- 1 = source
- 2 = gate
- 3 = drain

**PIN CONFIGURATION**



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### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	250 mA
Drain current (peak)	$I_{DM}$	max.	500 mA
Total power dissipation up to $T_{case} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	0.6 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

### THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	125 K/W
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### Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm × 10 mm.

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### CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified

Drain-source breakdown voltage

$$I_D = 10\ \mu\text{A}; V_{GS} = 0$$

$V_{(BR)DSS}$  min. 200 V

Drain-source leakage current

$$V_{DS} = 130\ \text{V}; V_{GS} = 0$$

$I_{DSS}$  max. 30 nA

Gate-source leakage current

$$V_{GS} = 15\ \text{V}; V_{DS} = 0$$

$I_{GSS}$  max. 10 nA

Gate threshold voltage

$$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$$

$V_{GS(th)}$  min. 1.0 V  
max. 3.0 V

Drain-source ON-resistance

$$I_D = 250\ \text{mA}; V_{GS} = 10\ \text{V}$$

$R_{DSon}$  typ. 4.5  $\Omega$   
max. 6.4  $\Omega$

$$I_D = 100\ \text{mA}; V_{GS} = 10\ \text{V}$$

$R_{DSon}$  typ. 4.2  $\Omega$   
max. 6.0  $\Omega$

Transfer admittance

$$I_D = 250\ \text{mA}; V_{DS} = 25\ \text{V}$$

$|y_{fs}|$  min. 200 mS  
typ. 350 mS

Input capacitance at  $f = 1\ \text{MHz}$

$$V_{DS} = 25\ \text{V}; V_{GS} = 0$$

$C_{iss}$  typ. 45 pF

Output capacitance at  $f = 1\ \text{MHz}$

$$V_{DS} = 25\ \text{V}; V_{GS} = 0$$

$C_{oss}$  typ. 15 pF

Feedback capacitance at  $f = 1\ \text{MHz}$

$$V_{DS} = 25\ \text{V}; V_{GS} = 0$$

$C_{rss}$  typ. 3.5 pF

Switching times (see Figs 2 and 3)

$$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V}; V_{GS} = 0\ \text{to}\ 10\ \text{V}$$

$t_{on}$  typ. 5 ns  
 $t_{off}$  typ. 15 ns

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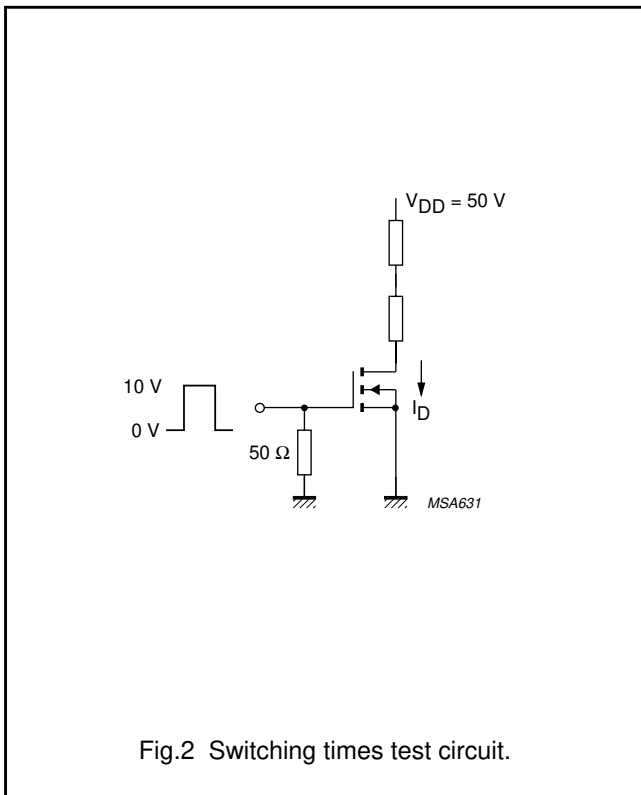


Fig.2 Switching times test circuit.

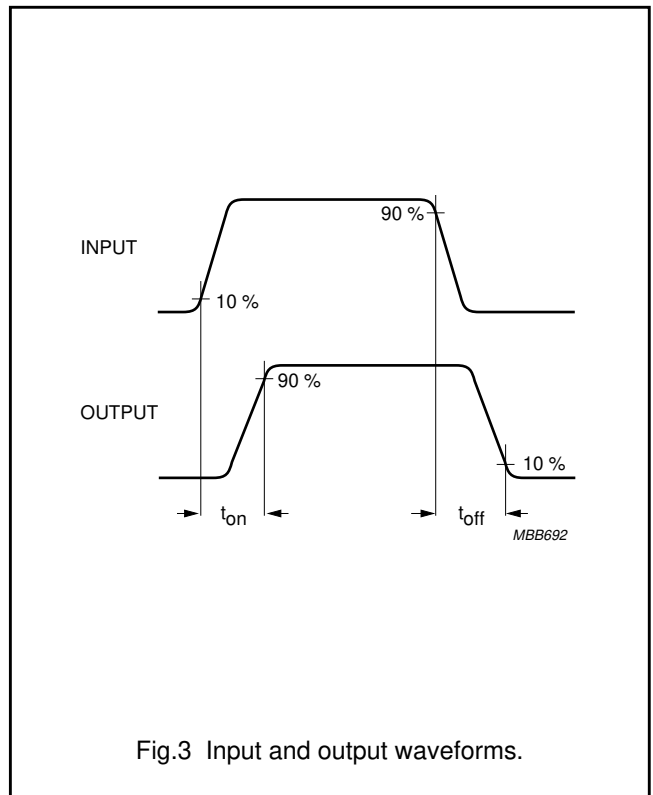


Fig.3 Input and output waveforms.

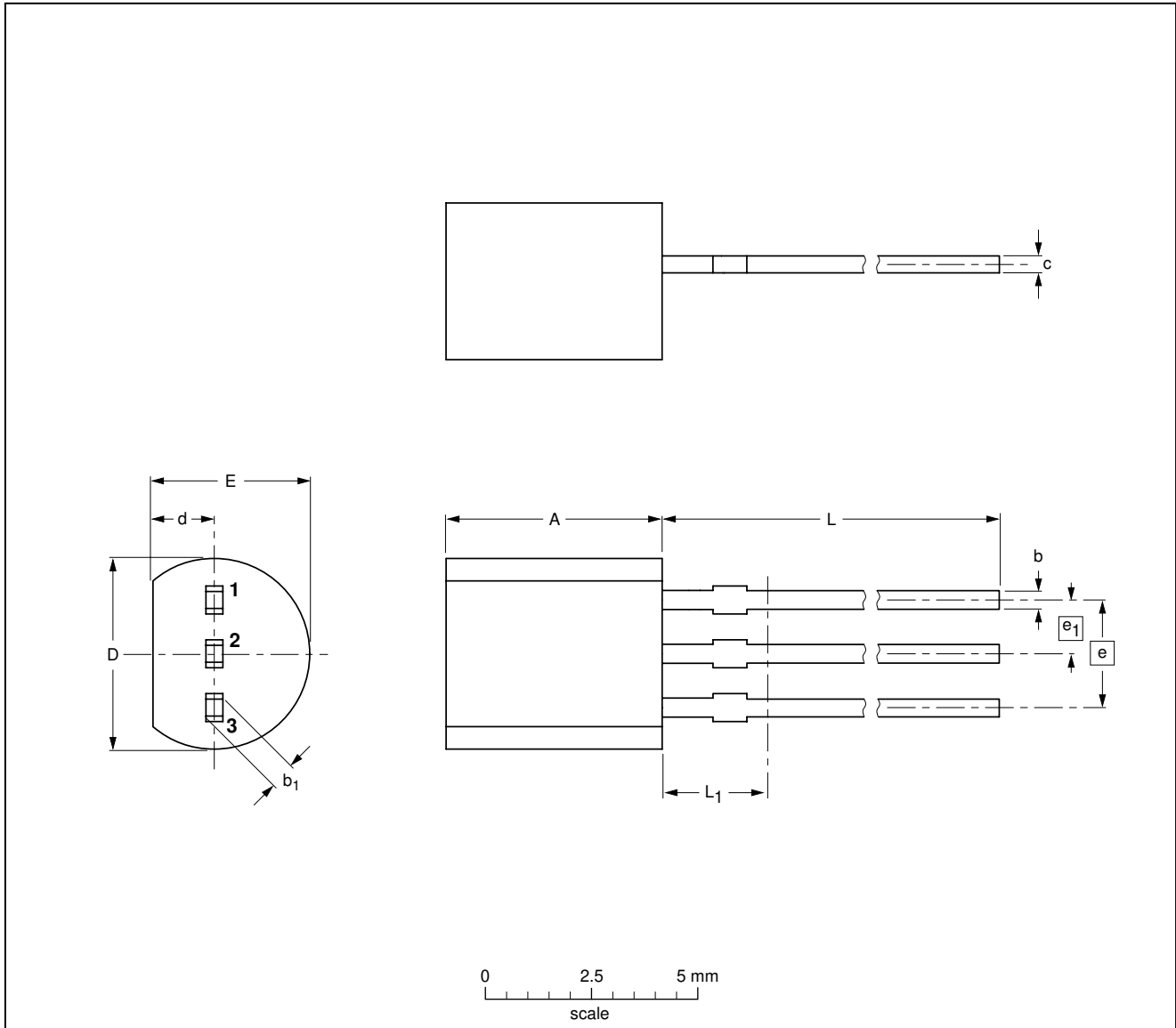
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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup>
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54		TO-92	SC-43		97-02-28

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## DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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