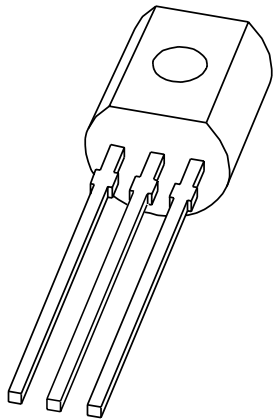


DATA SHEET



PSS8050

NPN medium power 25 V transistor

Product specification
Supersedes data of 2002 Nov 18

2004 Aug 10

NPN medium power 25 V transistor

PSS8050

FEATURES

- High total power dissipation
- High current capability.

APPLICATIONS

- Medium power switching and muting
- Amplification
- Portable radio output amplifier (class-B, push-pull).

DESCRIPTION

NPN transistor in a SOT54 (TO-92) plastic package.
PNP complement: PSS8550.

MARKING

TYPE NUMBER	MARKING CODE
PSS8050C	S8050C
PSS8050D	S8050D

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	25	V
I_C	collector current (DC)	1.5	A

PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter

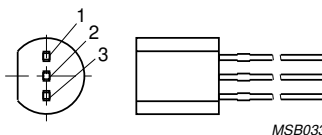


Fig.1 Simplified outline (SOT54).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	40	V
V_{CEO}	collector-emitter voltage	open base	–	25	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	collector current (DC)		–	1.5	A
I_{CM}	peak collector current		–	2	A
I_B	base current (DC)		–	300	mA
I_{BM}	peak base current		–	1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	850	mW
		$T_{amb} \leq 25\text{ °C}$; note 2	–	900	mW
		$T_{amb} \leq 25\text{ °C}$; note 3	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Device mounted on a printed-circuit board; single sided copper; tinplated; standard footprint.
2. Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector 1 cm².
3. Device mounted on a printed-circuit board; single sided copper; tinplated; standard footprint. Operated under pulsed conditions: pulse width $t_p \leq 1\text{ s}$; duty cycle $\delta \leq 0.75\%$.

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PSS8050

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; note 1	147	K/W
		in free air; note 2	139	K/W
		in free air; note 3	125	K/W

Notes

1. Device mounted on a printed-circuit board; single sided copper; tinplated; standard footprint.
2. Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector 1 cm².
3. Device mounted on a printed-circuit board; single sided copper; tinplated; standard footprint.
Operated under pulsed conditions: pulse width $t_p \leq 1$ s; duty cycle $\delta \leq 0.75\%$.

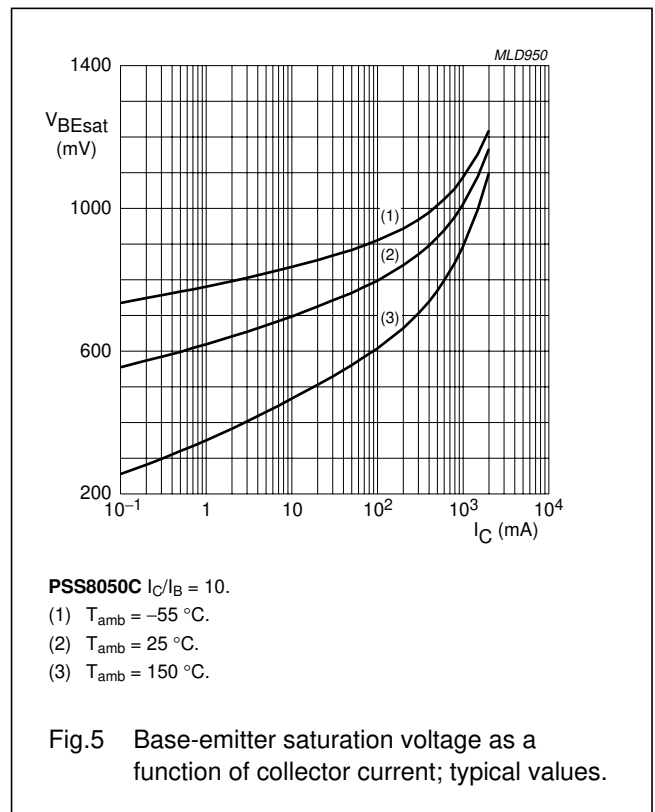
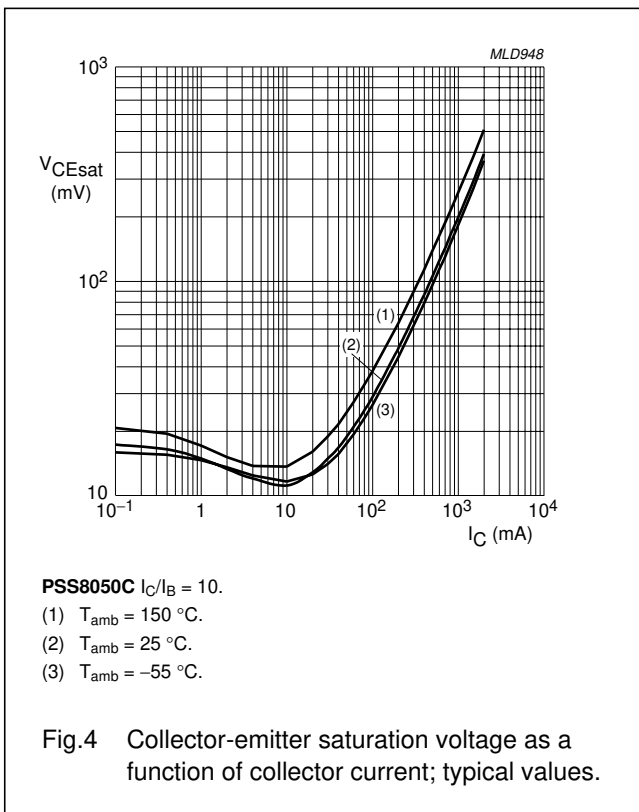
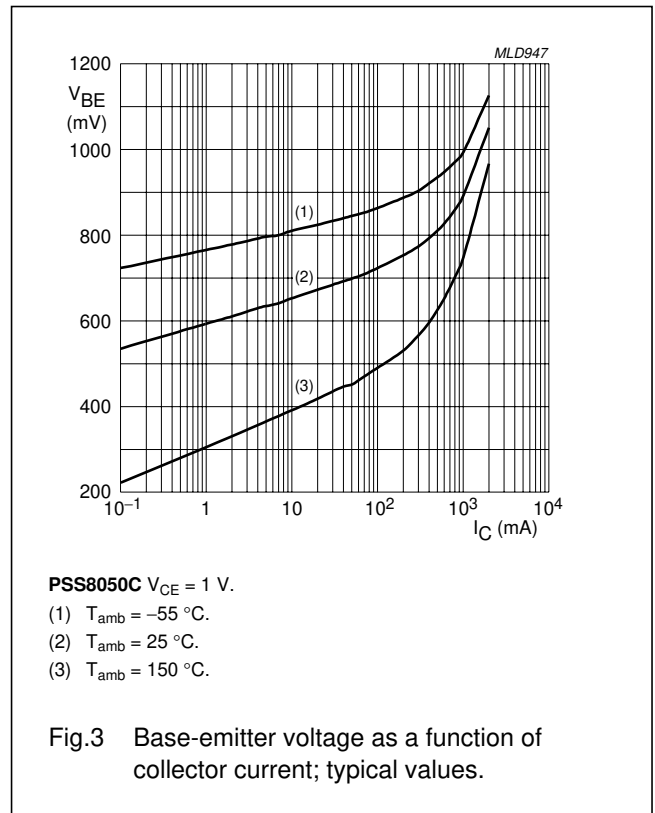
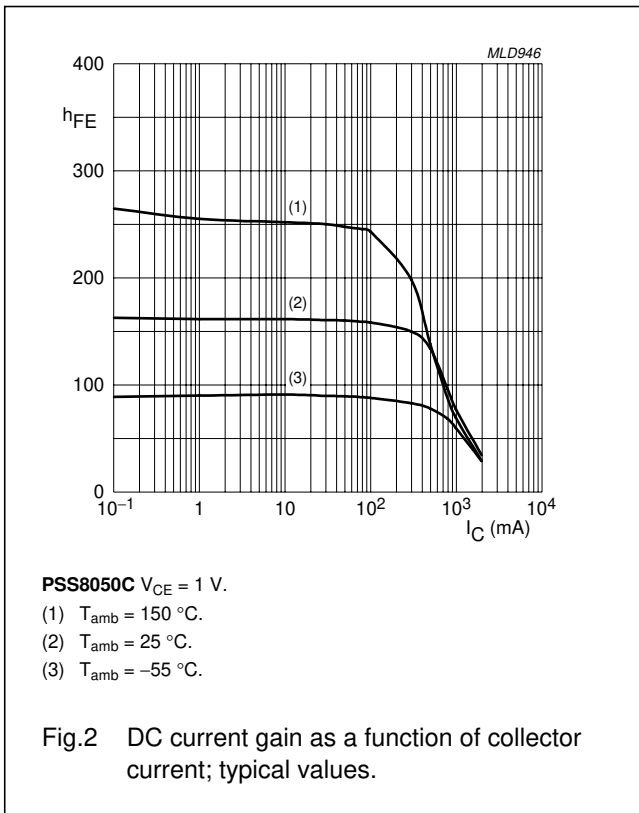
CHARACTERISTICS

$T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = 35$ V; $I_E = 0$	–	–	100	nA
		$V_{CB} = 35$ V; $I_E = 0$; $T_{amb} = 150$ °C	–	–	50	µA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 25$ V; $I_B = 0$	–	–	100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 6$ V; $I_C = 0$	–	–	100	nA
h_{FE}	DC current gain	$I_C = 5$ mA; $V_{CE} = 1$ V	45	–	–	
		$I_C = 800$ mA; $V_{CE} = 1$ V	40	–	–	
	DC current gain PSS8050C PSS8050D	$I_C = 100$ mA; $V_{CE} = 1$ V	120 160	– –	200 300	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 800$ mA; $I_B = 80$ mA	–	165	500	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 800$ mA; $I_B = 80$ mA	–	–	1.2	V
V_{BEon}	base-emitter turn-on voltage	$I_C = 10$ mA; $V_{CE} = 1$ V	–	–	1	V
f_T	transition frequency	$I_C = 50$ mA; $V_{CE} = 10$ V; $f = 100$ MHz	100	–	–	MHz
C_c	collector capacitance	$V_{CB} = 10$ V; $I_E = I_e = 0$; $f = 1$ MHz	–	–	10	pF

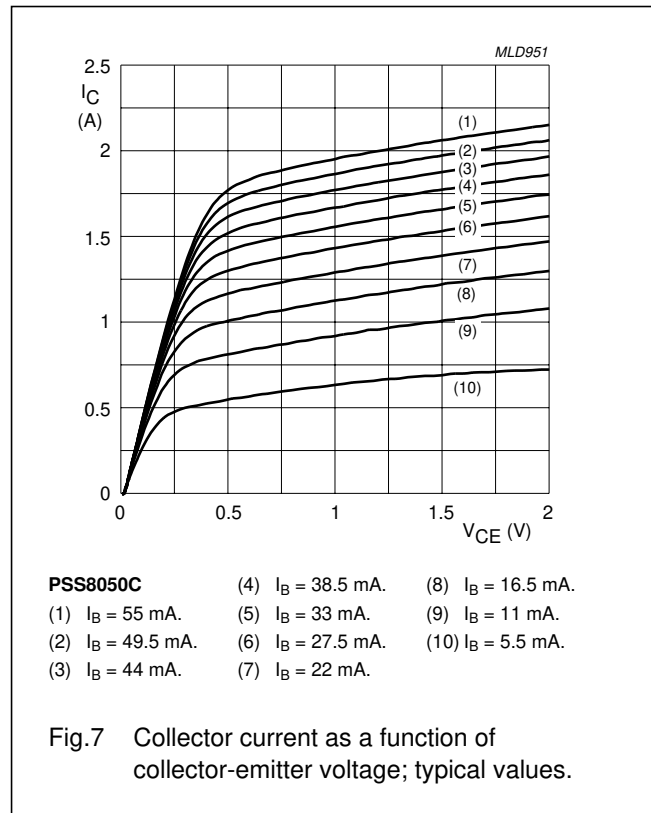
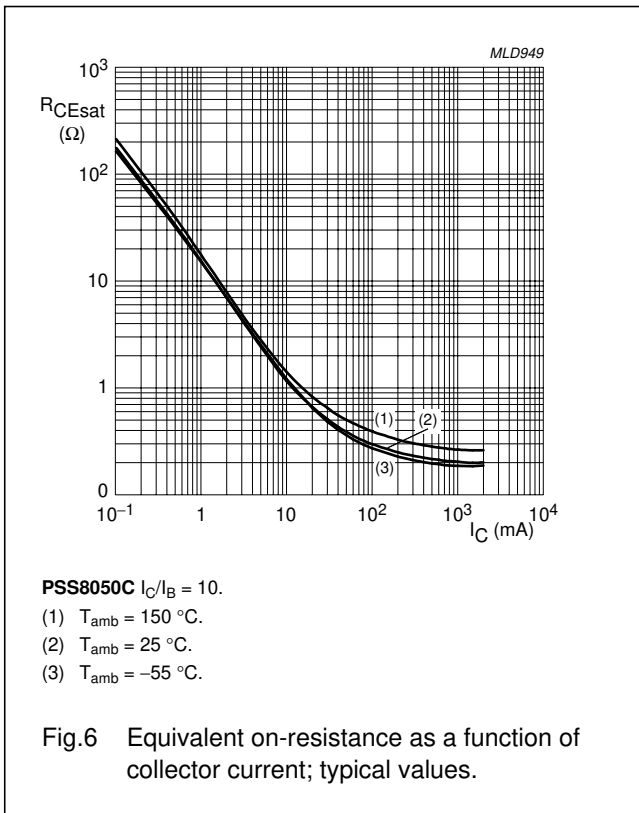
NPN medium power 25 V transistor

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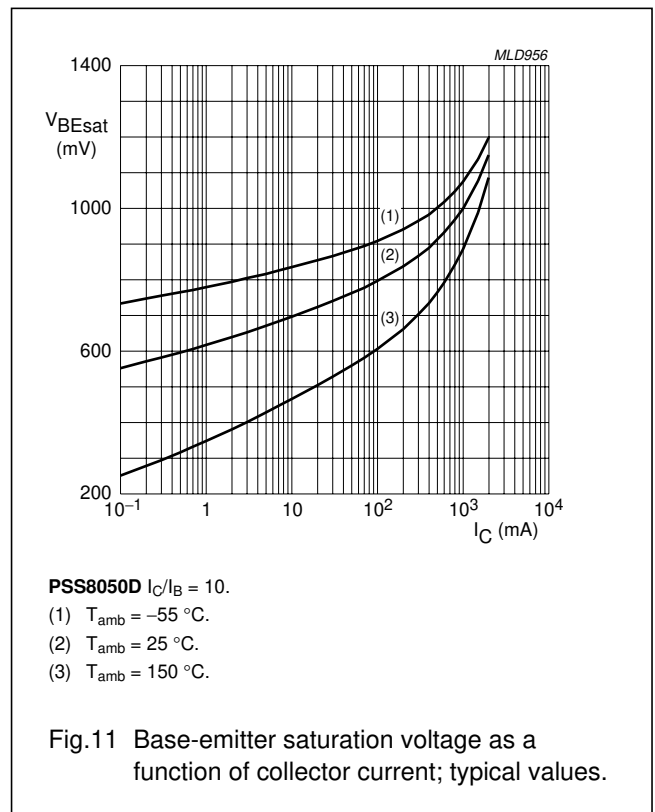
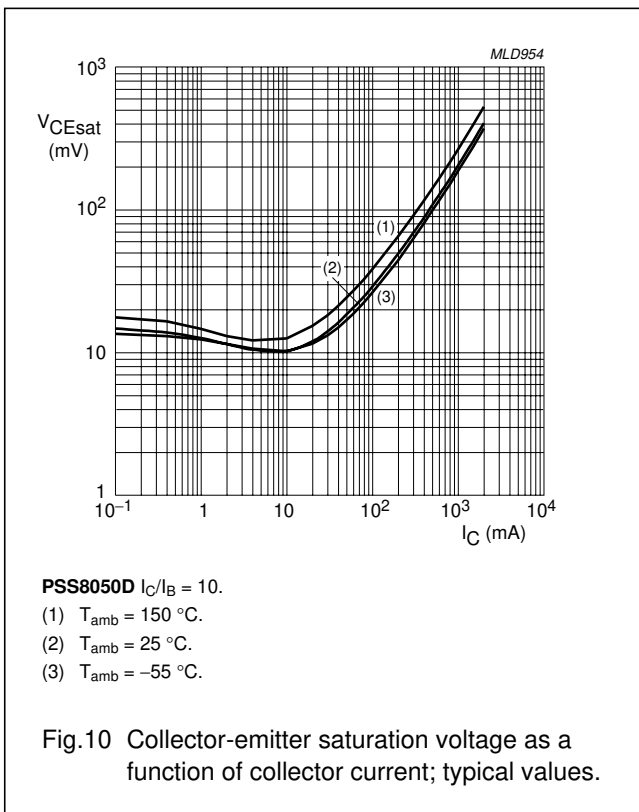
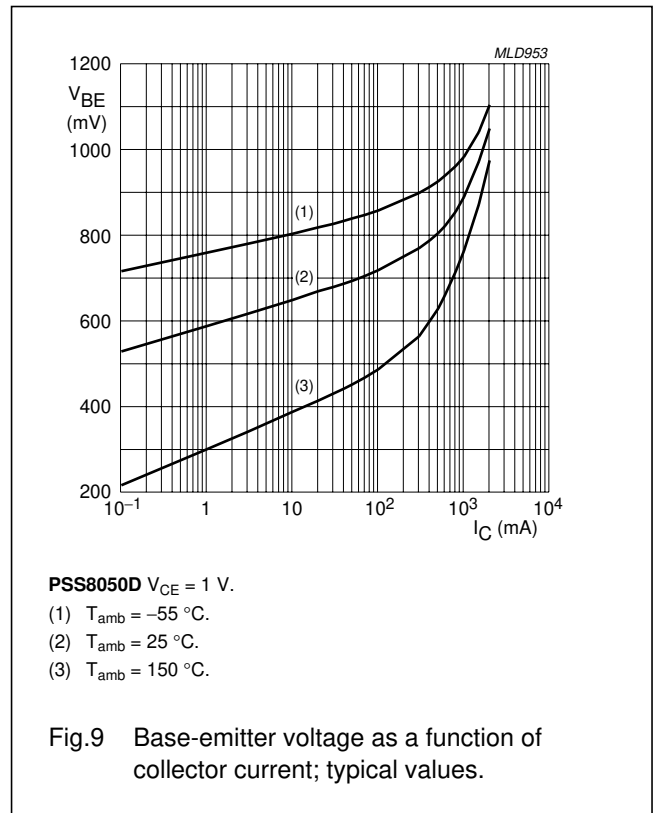
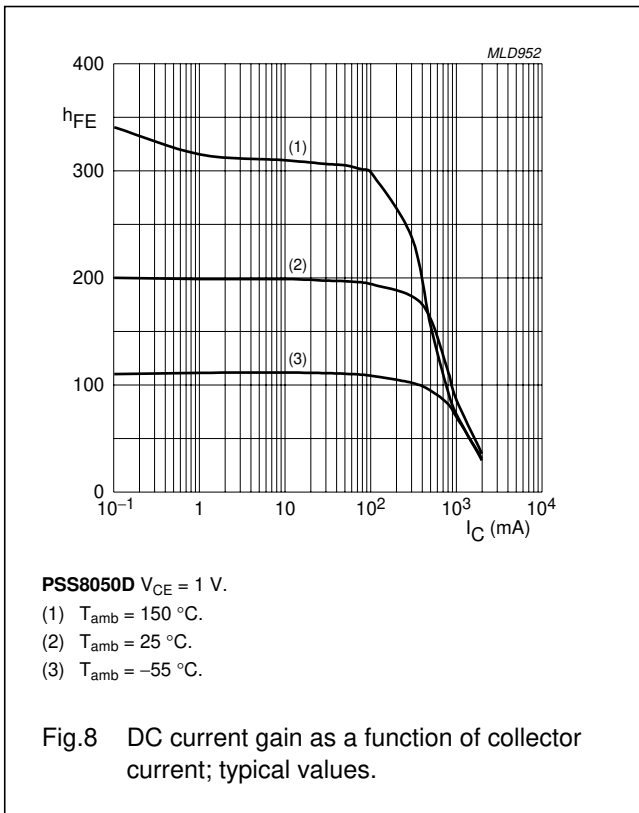
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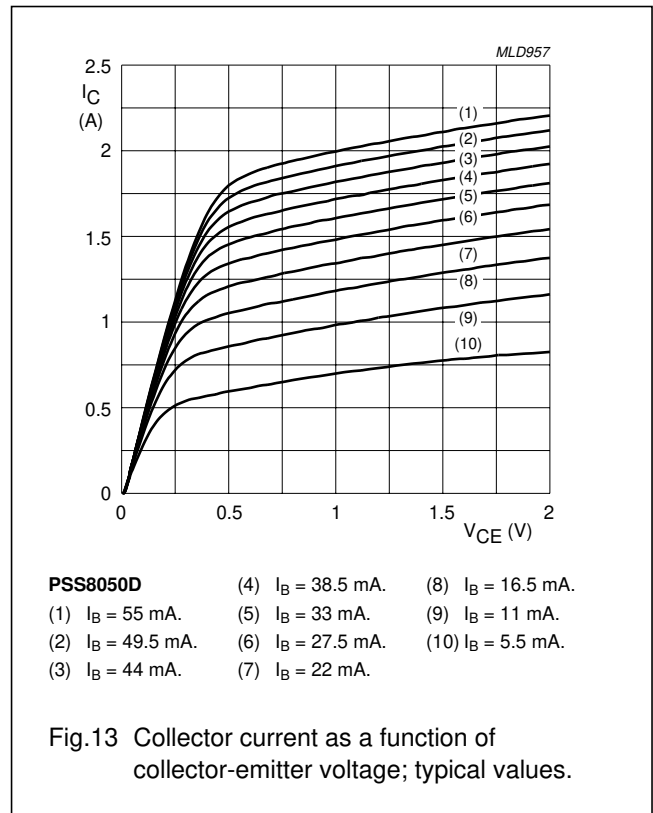
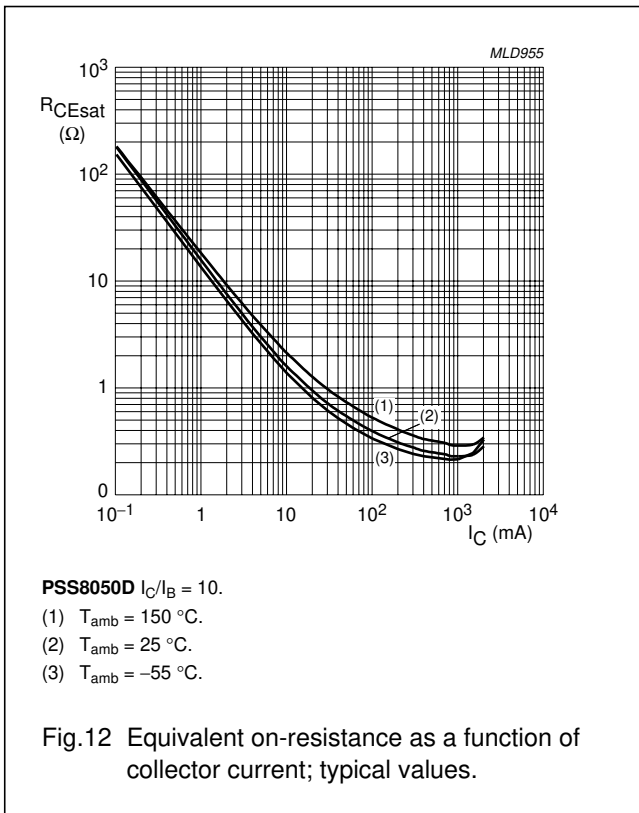
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NPN medium power 25 V transistor

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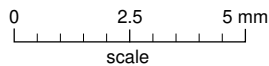
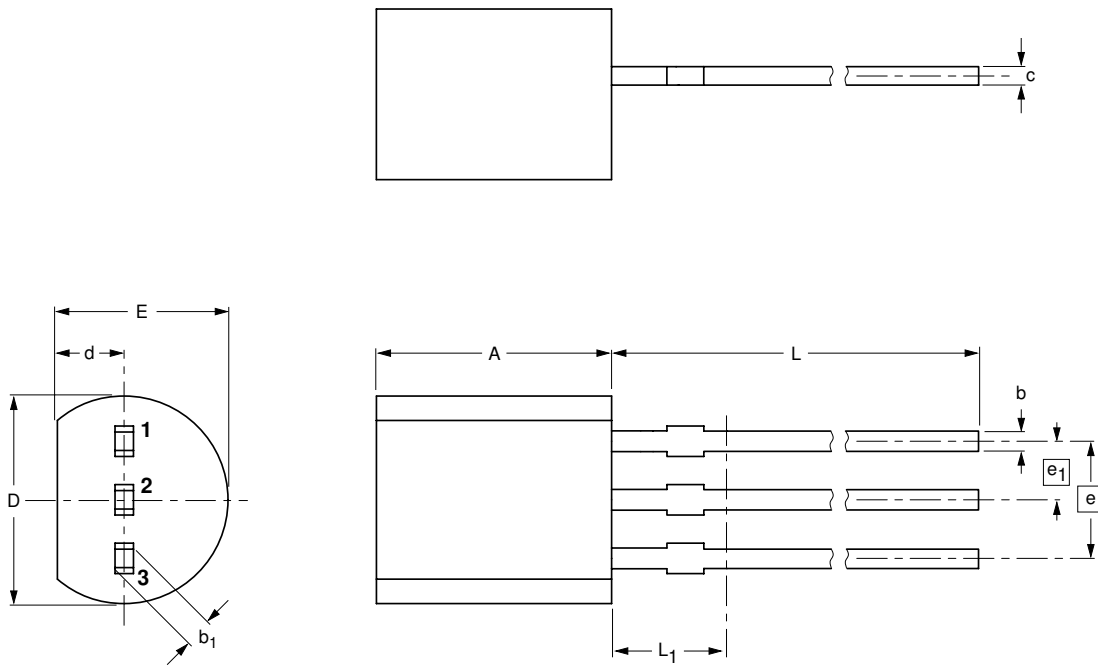
NPN medium power 25 V transistor

PSS8050

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		-97-02-28 04-06-28

NPN medium power 25 V transistor

PSS8050

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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