

Power driver IC for CD changer

BD7962FM

BD7962FM is a 6-channel driver (3-channel BTL driver + 3-channel loading driver) for car CD changer. This IC integrates 1-channel operational amplifier for various purposes. The size reduction of the set is achieved by integrating loading driver and actuator driver into a single chip.

●Applications

CD changer

●Features

- 1) This circuit is a 6-channel driver IC consisting of three BTL drivers and three loading drivers.
- 2) Two wide dynamic range loading drivers of MOS output ($R_{ON}=1.0\Omega$).
- 3) The circuit is provided with loading driver voltage setting terminals.
- 4) A general Opamp and Pre Opamp are built in.
- 5) The circuit has a mute switch.
- 6) The circuit has a reset terminal.
- 7) A thermal shutdown circuit is built in.
- 8) Since HSOP-M36 power package is used, the set requires a reduced space.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V _{cc}	15	V
Power dissipation	P _d	2.2*	W
Operating temperature range	T _{opr}	-40 to +85	°C
Storage temperature range	T _{stg}	-55 to +150	°C

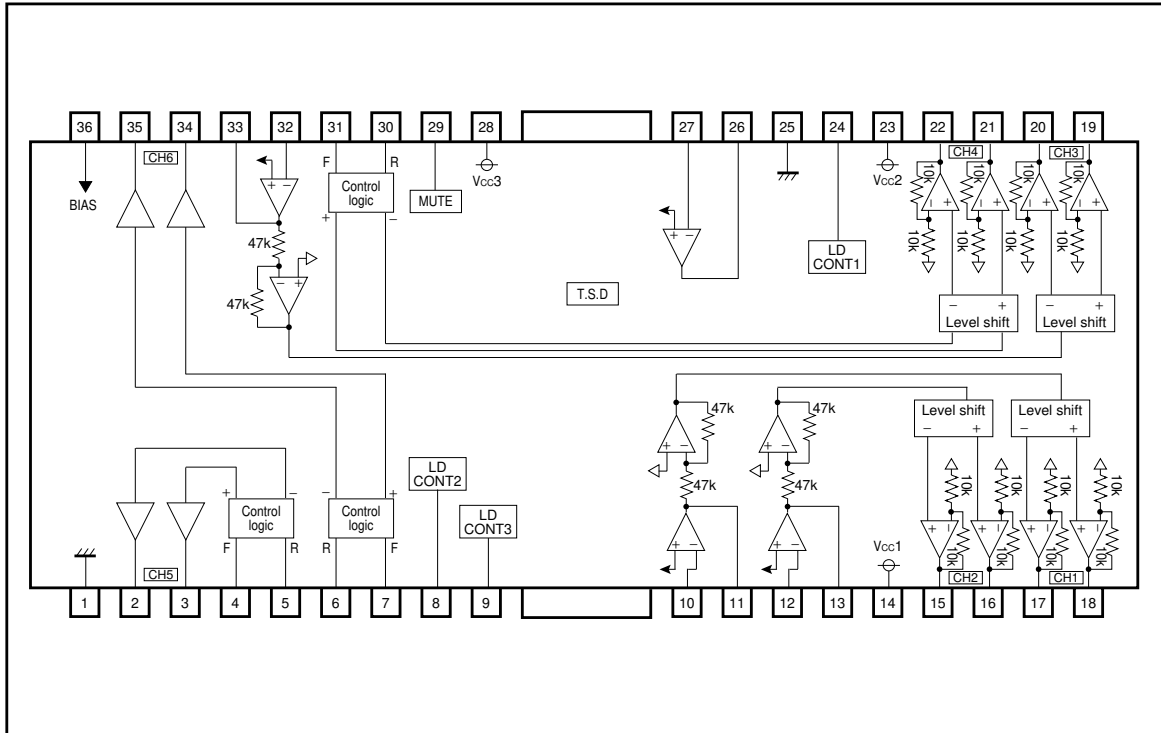
* Reduced by 17.6mW for each increase in Ta of 1°C over 25°C, on less than 3% (percentage occupied by copper foil), 70mm×70mm, t=1.6mm, glass epoxy mounting.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage 1 (CH1, CH2)	V _{cc1}	4.5	5.0	V _{cc3}	V
Supply voltage 2 (CH3, CH4)	V _{cc2}	4.5	8.0	14.0	V
Supply voltage 3 (CH5, CH6)	V _{cc3}	4.5	8.0	14.0	V

Optical disc ICs

●Block diagram



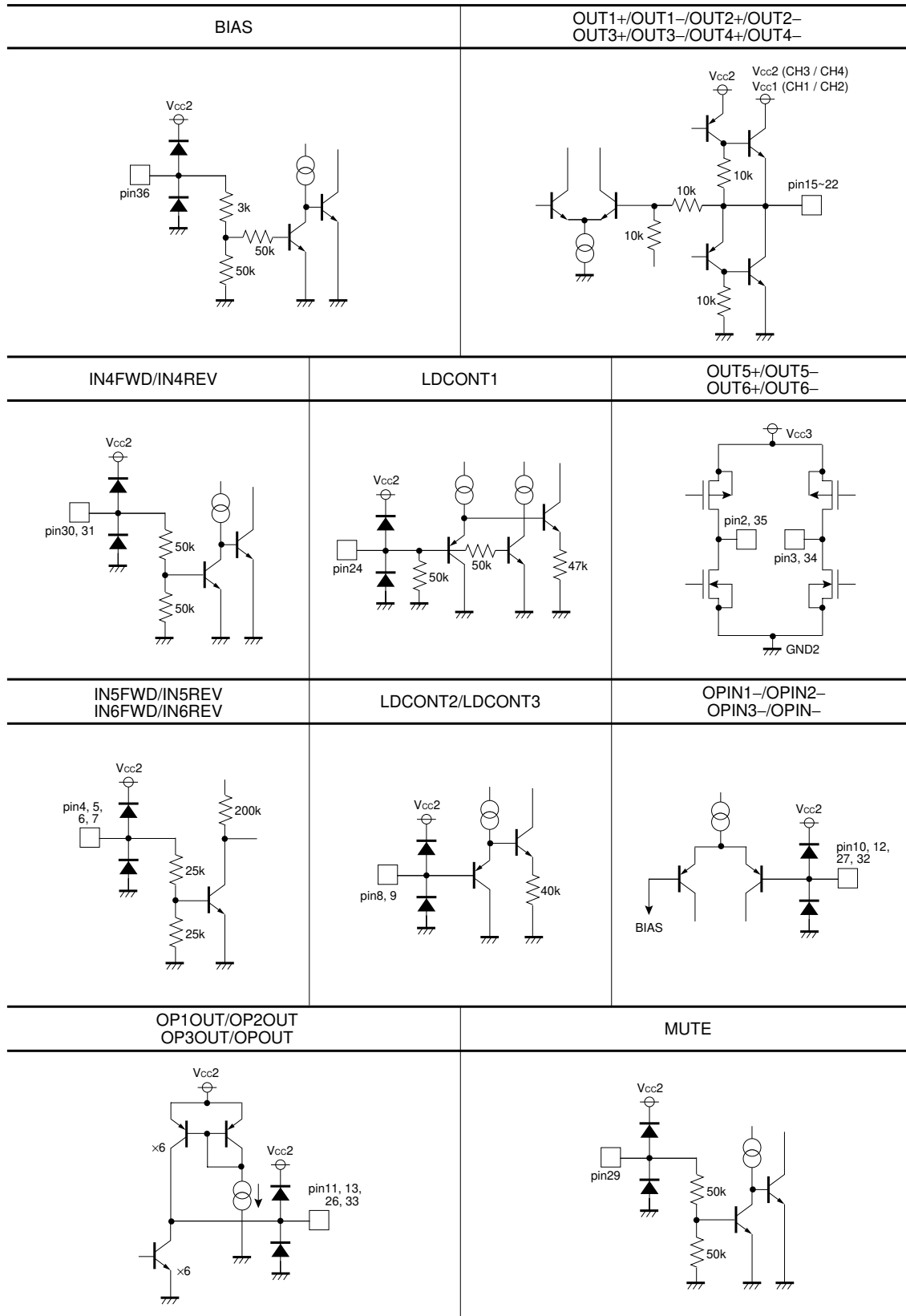
●Pin descriptions

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	GND2	POW GND (loading driver unit)	19	OUT3+	BTL driver (CH3) output +
2	OUT5-	Loading driver (CH5) output -	20	OUT3-	BTL driver (CH3) output -
3	OUT5+	Loading driver (CH5) output +	21	OUT4+	Loading driver (CH4) input +
4	IN5FWD	Loading driver (CH5) FWD input	22	OUT4-	Loading driver (CH4) input -
5	IN5REV	Loading driver (CH5) REV input	23	Vcc2	Supply voltage (CH3, CH4)
6	IN6REV	Loading driver (CH6) REV input	24	LDCONT1	Loading driver (CH4) voltage setting terminal
7	IN6FWD	Loading driver (CH6) FWD input	25	GND1	POW GND (BTL driver unit)
8	LDCONT2	Loading driver (CH5) voltage setting terminal	26	OPOUT	Opamp output
9	LDCONT3	Loading driver (CH6) voltage setting terminal	27	OPIN-	Opamp negative input
10	OPIN1-	CH1 opamp negative input	28	Vcc3	Supply voltage (CH5, CH6)
11	OP1OUT	CH1 opamp output	29	MUTE	BTL driver mute terminal
12	OPIN2-	CH2 opamp negative input	30	IN4REV	Loading driver (CH4) REV input
13	OP2OUT	CH2 opamp output	31	IN4FWD	Loading driver (CH4) FWD input
14	Vcc1	Supply voltage (CH1, CH2)	32	OPIN3-	CH3 opamp negative input
15	OUT2-	BTL driver (CH2) output -	33	OP3OUT	CH3 opamp output
16	OUT2+	BTL driver (CH2) output +	34	OUT6+	Loading driver (CH6) output +
17	OUT1-	BTL driver (CH1) output -	35	OUT6-	Loading driver (CH6) output -
18	OUT1+	BTL driver (CH1) output +	36	BIAS	BIAS terminal

* Symbol of + and - (output of BTL driver) means polarity to opamp output pin.
For example if Opamp output voltage is H, BTL driver +output is H, -output is L

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●Input output circuit



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●Electrical characteristics

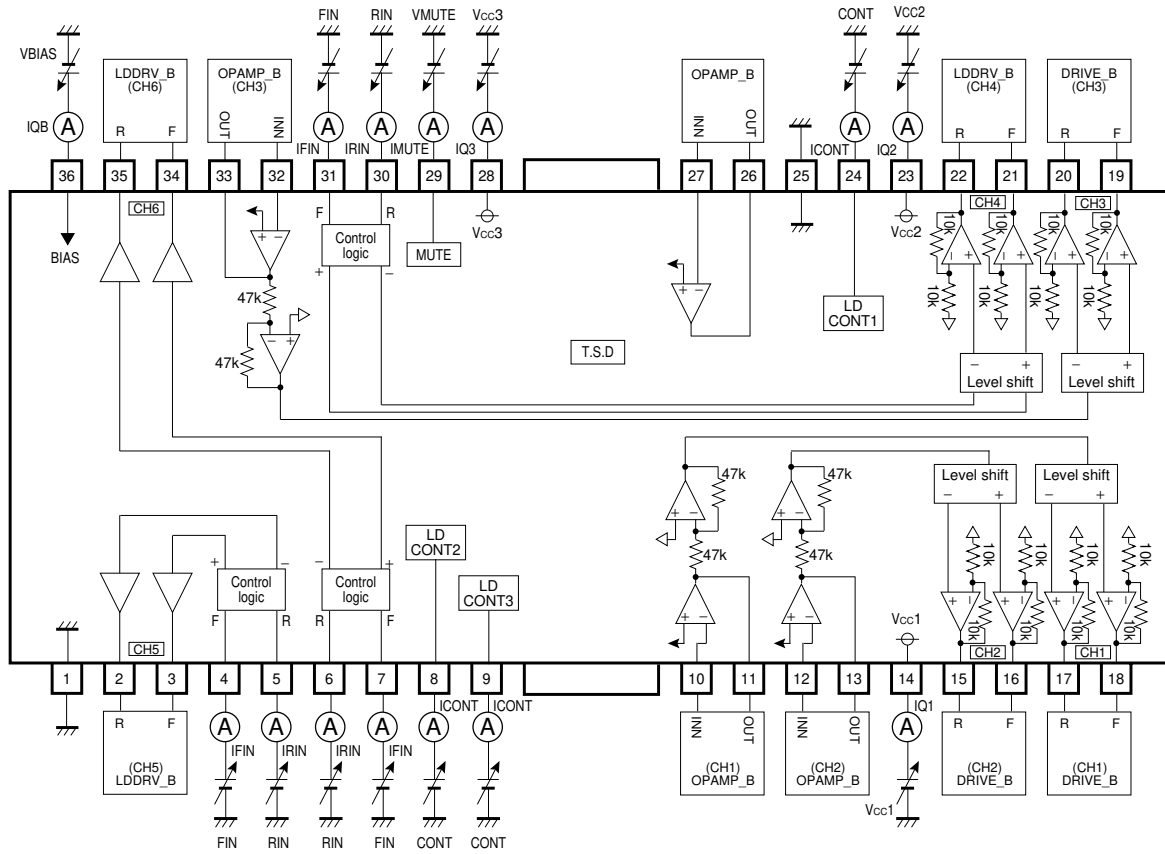
(unless otherwise noted, $T_a=25^\circ\text{C}$, $V_{CC1}=5\text{V}$, $V_{CC2}=V_{CC3}=8\text{V}$, $\text{BIAS}=1.65\text{V}$, $R_L=8\Omega$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current (Vcc1)	Icc1	–	0.30	0.70	mA	Under no load
Quiescent current (Vcc2)	Icc2	11.5	23	32	mA	Under no load
Quiescent current (Vcc3)	Icc3	1.9	3.8	5.7	mA	Under no load
〈 BTL driver CH1 to CH3 〉						
Output offset voltage	V _{OFS}	–40	0	+70	mV	
Max. output amplitude (CH1, CH2)	V _{OM1}	3.7	4.0	–	V	
Max. output amplitude (CH3)	V _{OM2}	5.4	6.0	–	V	
Closed circuit voltage gain	G _{VC}	10	12	14	dB	V _{IN} =BIAS±0.5V Opamp : Buffer
Mute terminal sink current	I _{MUTE}	–	80	125	μA	VMUTE=5V
Bias terminal sink current	I _{BIAS}	–	75	120	μA	VBIAS=2.5V
〈 Loading driver CH4 to CH6 〉						
Output offset voltage	V _{OFSL}	–35	0	+35	mV	When brake is applied
Max. output amplitude (CH4)	V _{OML}	5.4	6.0	–	V	R _L =8Ω
Output saturation voltage H (CH5, CH6)	V _{OLH}	–	0.38	0.70	V	I _o =500mA
Output saturation voltage L (CH5, CH6)	V _{OLL}	–	0.12	0.25	V	I _o =500mA
Voltage gain	G _{VLD}	4.0	6.0	8.0	dB	LDCONT=1V
Input terminal sink current	I _{INL}	–	180	270	μA	LDIN=5V
LDCONT terminal source current (LDCONT1)	I _{LDC1}	–	–	0.5	mA	LDCONT=5V
LDCONT terminal source current (LDCONT2, 3)	I _{LDC2}	–	–	300	nA	LDCONT=5V
〈 Opamp and Pre opamp CH1 to CH3 〉						
Input offset voltage	V _{OPOFS}	–5	0	5	mV	
Input bias current	I _{OPIB}	–	–	300	nA	
Common mode input voltage range	V _{OPICM}	0.3	–	V _{CC} –1.2	V	
Maximum output source current	I _{SOURCE}	500	800	–	μA	
Maximum output sink current	I _{SINK}	2	–	–	mA	
Slew rate	SR	–	2	–	V/μs	

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● Measurement circuits



The resistance values are indicated in Ω.

Fig.1

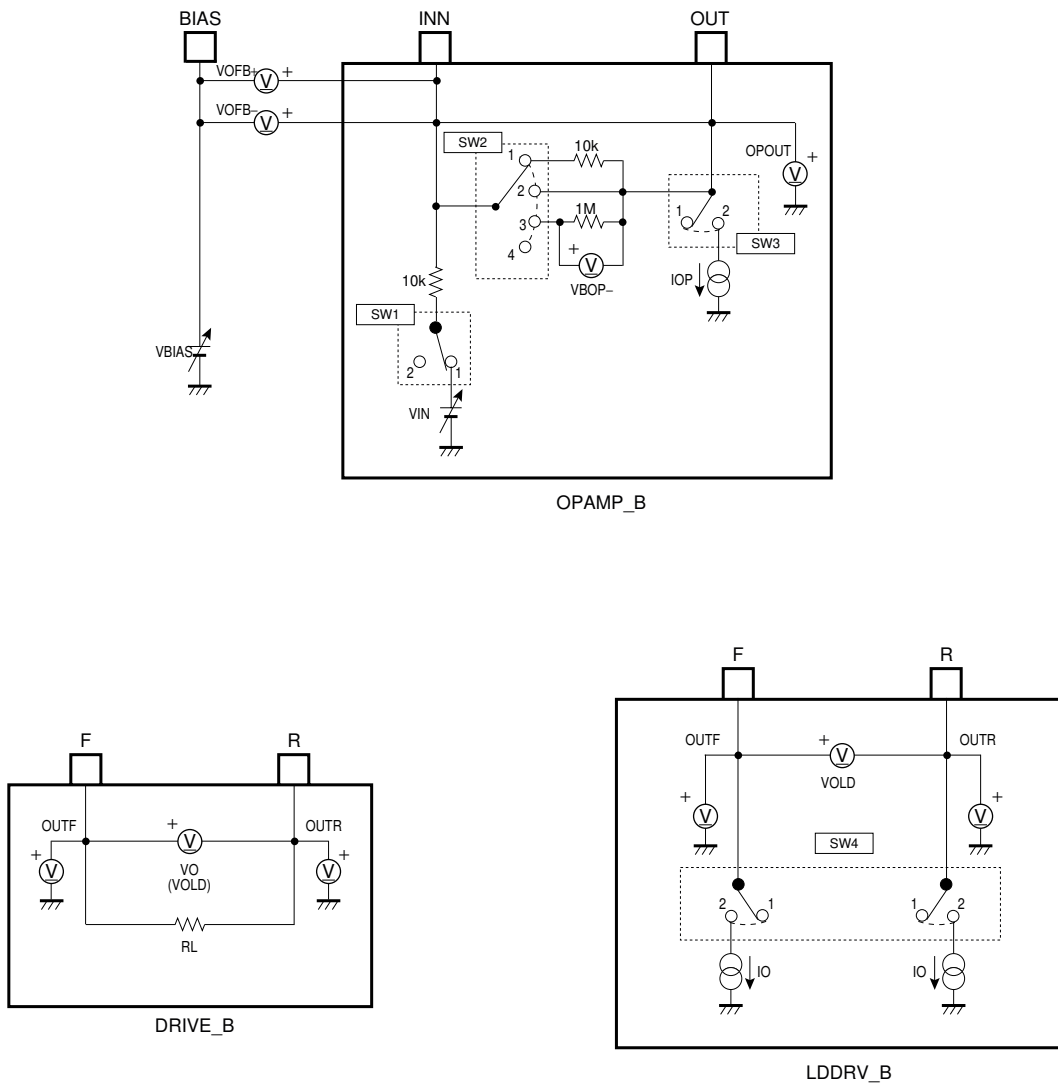


Fig.2

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●Switch table for measuring circuit diagrams

(unless otherwise noted, $T_a=25^\circ\text{C}$, $V_{CC1}=5\text{V}$, $V_{CC2}=V_{CC3}=8\text{V}$, $\text{BIAS}=1.65\text{V}$, $R_L=8\Omega$ Unless otherwise specified, the switch 1 is used.)

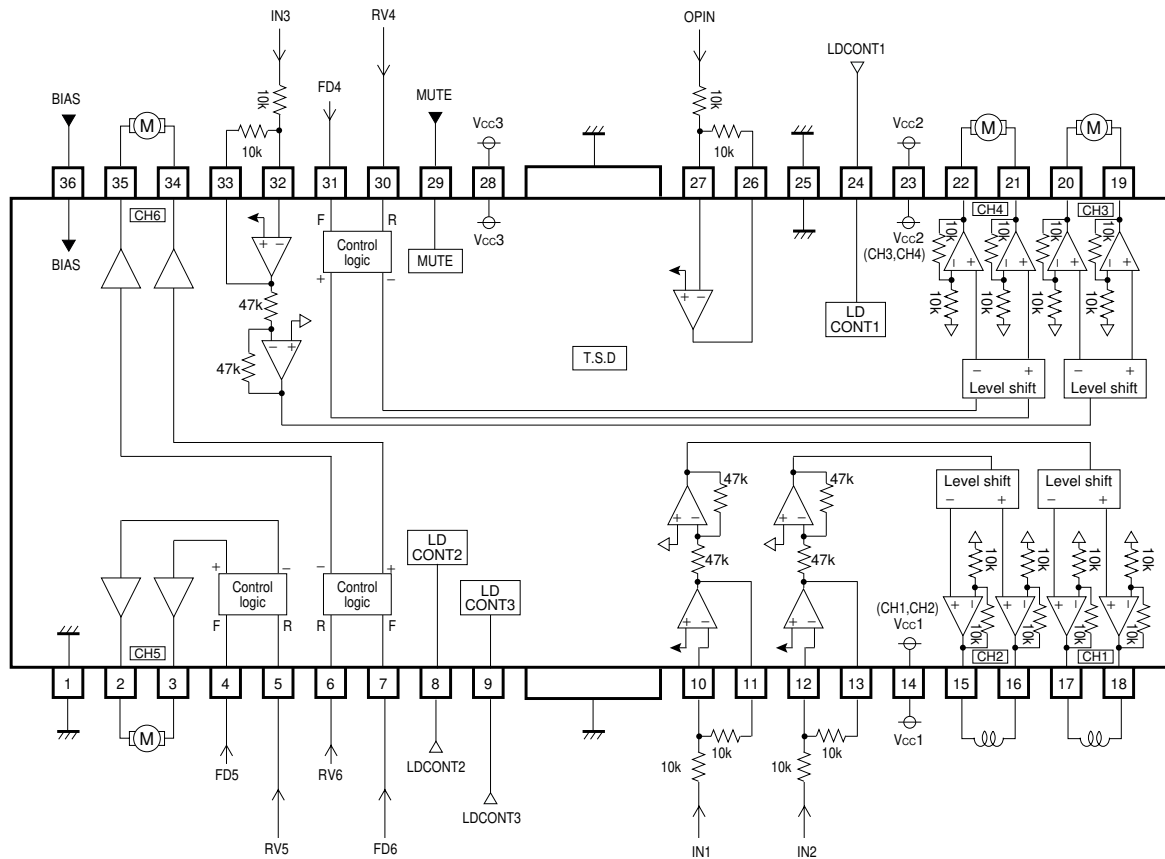
Parameter	Symbol	Switching				Conditions	Measurement circuit
		1	2	3	4		
Quiescent current (V_{CC1})	I_{CC1}	2				Under no load	Fig.1, 2
Quiescent current (V_{CC2})	I_{CC2}	2				Under no load	Fig.1, 2
Quiescent current (V_{CC3})	I_{CC3}	2				Under no load	Fig.1, 2
(BTLdriver CH1 to CH3)							
Output offset voltage	V_{OFS}	2				$V_{OFS}=V_O$	Fig.1, 2
Max. output amplitud (CH1, CH2)	V_{OM1}					$V_{IN}=GND$, $V_{OM1}=V_O$	Fig.1, 2
Max. output amplitud (CH3)	V_{OM2}					$V_{IN}=GND$, $V_{OM1}=V_O$	Fig.1, 2
Closed circuit voltage gain(CH1 to CH3)	G_{VC}		2			$V_{IN}=VB\pm 0.5V$, $G_{VC}=20\log(V_O/0.5)$	Fig.1, 2
Difference between positive and negative voltage gains (CH1 to CH3)	ΔG_{VC}						Fig.1, 2
Mute terminal sink current	I_{MUTE}					$V_{MUTE}=5V$, $I_{MUTE}=I_{MUTE}$	Fig.1, 2
Bias terminal sink current	I_{BIAS}					$V_B=2.5V$, $I_{BIAS}=I_B$	Fig.1, 2
(Loading driver CH4 to CH6)							
Output offset voltage	V_{OFSL}					$F_{IN}=R_{IN}=5V$, $V_{OFSL}=V_{OLD}$	Fig.1, 2
Max. output amplitud (CH4)	V_{OML}					$F_{IN}=5V$, $R_{IN}=0V$, $V_{OML}=L_{OLD}$	Fig.1, 2
Output saturation voltage H (CH5, 6)	V_{OLH}				2	$I_O=500\text{mA}^{*1}$	Fig.1, 2
Output saturation voltage L (CH5, 6)	V_{OLL}				2	$I_O=500\text{mA}^{*2}$	Fig.1, 2
Voltage gain (Loading)	G_{VLD}					$CONT=1V$, $G_{VLD}=20\log(V_{OLD}/1V)$	Fig.1, 2
Difference between positive and negative voltage gains (Loading)	ΔG_{VLD}						Fig.1, 2
Input terminal sink current	I_{INL}					$F_{IN}=R_{IN}=5V$, $I_{INL}=I_{FIN}$, I_{RIN}	Fig.1, 2
LDCONT terminal source current	I_{LDC}					$CONT=5V$, $I_{LDC}=I_{CONT}$	Fig.1, 2
(Opamp and Pre opamp CH1 to CH3)							
Input offset voltage	V_{OPOFS}	2				$V_{OPOFS}=V_{OFB+}$	Fig.1, 2
Input bias current	I_{OPIB}	2	3			$I_{OPIB}=V_{BOP}/1M\Omega$	Fig.1, 2
Common mode input voltage range	V_{OPICM}		2			$V_{OPICM} : V_{IN}=OPOUT$ range	Fig.1, 2
Max. output source current	I_{SOURCE}	2	2	2			Fig.1, 2
Max. output sink current	I_{SINK}	2	2	2			Fig.1, 2
Slew rate	SR		2			$V_{IN}=f : 100\text{kHz}$, 1V to 3V pulse	Fig.1, 2

*1 $F_{IN}=5V$, $R_{IN}=0V$, $V_{OLH}=V_{CC}-OUT+$
 $F_{IN}=0V$, $R_{IN}=5V$, $V_{OLH}=V_{CC}-OUT-$

*2 $F_{IN}=5V$, $R_{IN}=0V$, $V_{OLL}=OUT-$
 $F_{IN}=0V$, $R_{IN}=5V$, $V_{OLL}=OUT+$

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●Application example



The resistance values are indicated in Ω .

Fig.3

●Operation notes

- (1) BD7962FM has a built-in thermal shutdown circuit.
When the chip temperature reaches 175°C (Typ.), the output current from all drivers is muted.
When the chip temperature returns to 150°C (Typ.), the circuit of the driver unit starts up.
- (2) When the mute terminal (pin29) is opened or the terminal voltage is reduced to 0.5V or less, the output current of the BTL driver (CH1~CH3) unit is muted.
In the normal state of use, pull up the voltage to 2.0V or more.
- (3) When the bias terminal (pin36) voltage is reduced to 0.7V or less, the BTL driver (CH1~CH3) unit is muted.
In the normal state of use, set the voltage to 1.1V or more.
- (4) Thermal shutdown mutes all drivers. When the mute ON voltage and the bias terminal voltage are reduced, only the BTL drivers are muted. But Opamp are not muted by all condition.
When the drivers are muted, the BTL driver (CH1, CH2) output terminal voltage becomes the internal bias voltage $V_{cc1}/2V$ and the BTL driver (CH3) output terminal voltage become the internal bias voltage $(V_{cc2}-0.7)/2V$.

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(5) The loading drivers operate according to the following logic.

INPUT		OUTPUT		Function
FWD	REV	OUT+	OUT-	
L	L	Hi Z	Hi Z	High impedance
L	H	L	H	REV mode
H	L	H	L	FED mode
H	H	L	L	Brake mode

The output voltage can be changed by adjusting the voltage input to the LDCONT terminal (gain of 6dB Typ.). However, even if the input voltage is increased excessively, the output voltage will not exceed the max. output voltage that depends on the supply voltage.

When the LDCONT terminal (pin 8, 9, 24) voltage is reduced to 0.7V or less, the loading driver is High impedance mode. But loading driver (CH4) output terminal voltage becomes the internal bias voltage ($V_{CC1}-0.7$)/2V.

(6) Supply voltage of V_{CC2} (pin23) should be equal to or higher than V_{CC1} (pin14) and V_{CC3} (pin28). Insert by the pass capacitor (approx. 0.1 μ F) between V_{CC} pin and GND pin of IC as near as possible.

(7) Connect the radiating fin with external GND.

(8) Output pin is to avoid short-circuit with V_{CC} , GND and other output pins. An integrated circuit is damaged, and smoke may come out by the case.

●Electrical characteristic curves

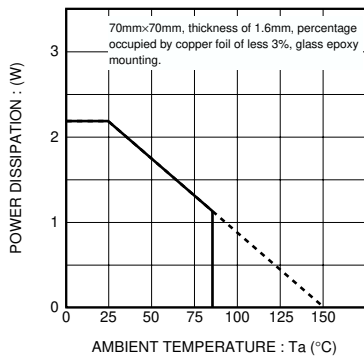


Fig.4 Power dissipation

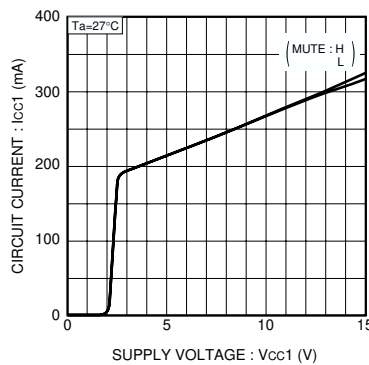


Fig.5 Circuit current characteristic Vcc1

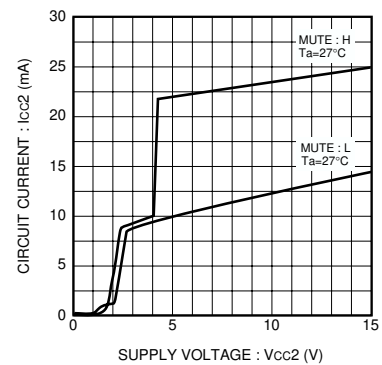


Fig.6 Circuit current characteristic Vcc2

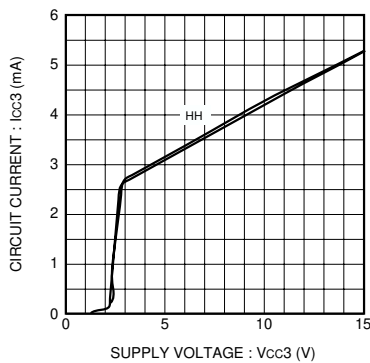


Fig.7 Circuit current characteristic Vcc3

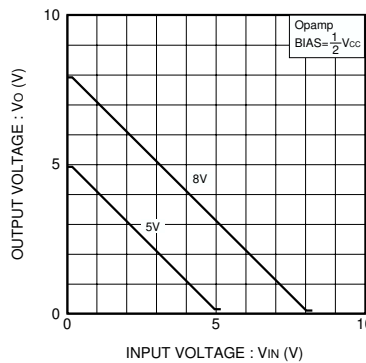


Fig.8 Input output characteristic

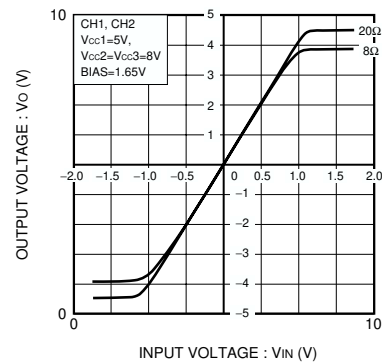


Fig.9 Input output characteristic

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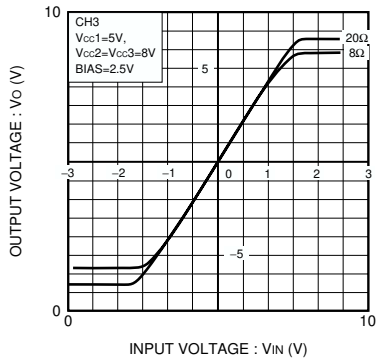


Fig.10 Input output characteristic

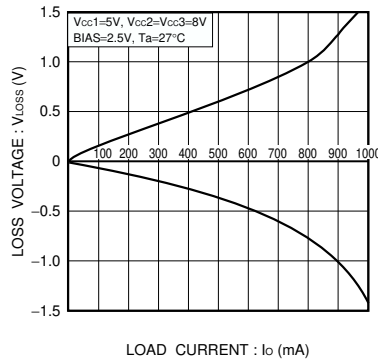


Fig.11 Output load current regulation

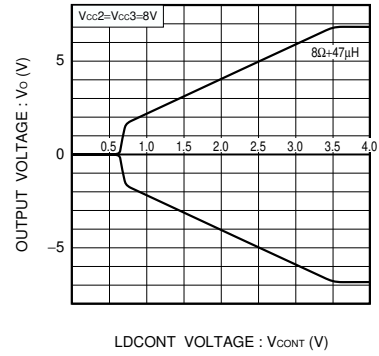


Fig.12 Input output characteristic

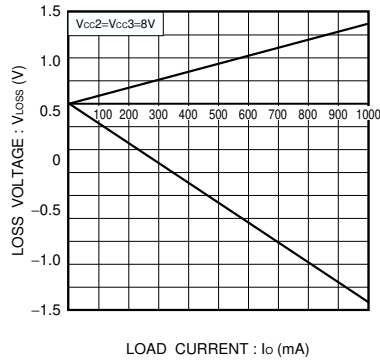
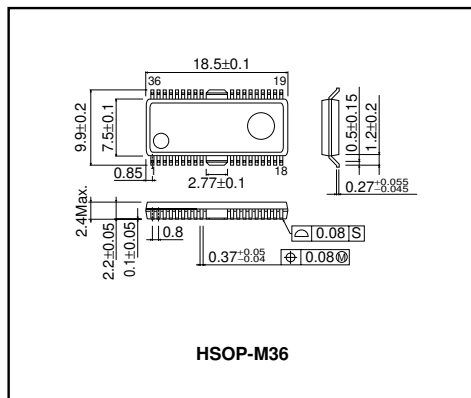


Fig.13 Output load current regulation

●External dimensions (Units : mm)



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